
**PAS 2080/DIO
ENGINEERING SPECIFICATION**

**32 CHANNEL CHANGE OF STATE AND
8 TTE PATTERN GENERATOR CARD
REVISION A (08/04/2003)**

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32 CHANNEL CHANGE OF STATE AND 8 TTE PATTERN GENERATOR CARD

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I. INTRODUCTION

GENERAL DESCRIPTION

The PAS 2080/DIO is a PCI based, 32 channel Change Of State, (COS), detector and 8 channel, Time To Edge, (TTE), pattern generator with 1 uSec resolution. Separate input and output FIFO's are provided to elastically buffer the input and output data patterns from the PCI bus. A 40 bit , 1 MHz counter that can be set and enabled from the PCI bus is also provided to time stamp the input data, and to determine when the output patterns are updated.

In order to generate output data patterns, time and output data values that represent the pattern to be generated are loaded from the PCI bus into the output FIFO. When the card is enabled, the first time value in the FIFO will be monitored until it matches the value of the 40-bit counter. Upon occurrence of the time match, the output data pattern will be presented to the card's output drivers, and the next time value in the FIFO will be compared to the value of the counter. The FIFO is 2,048 words deep by 32 bits wide. Storing the 40-bit time value and eight bits of output data requires two locations in the output FIFO, and allows 1,024 time and data value pairs to be stored.

Each time a change of state is detected on the input lines, the card will store the state of the 32 input signals and the associated time value in the input FIFO. When interrupts are enabled, a PCI interrupt will be generated any time the FIFO is empty and a change of state occurs causing new data to be loaded into the input FIFO. Storing the 40-bit time value and 32 bits of input data requires three locations in the input FIFO. This allows 682 time and data value pairs to be stored in the input FIFO.

The eight output signals use RS-232 voltage levels and the 32 input signals use TTL levels. A 100-pin connector mounted through the front panel provides access to the input and output signals. A board identifier, and control and status register are provided in addition to the 40-bit, 1 uSec counter and the input and output FIFOs.

Card Features: PAS 2080/DIO

- Eight RS- 232 voltage level output signals, 32 TTL compatible input channels
- Input and output signals terminate on a 100-pin connector at the front panel.
- On board Output FIFO stores output data pattern and time stamp. This FIFO is 32 bits wide by 2,048 words deep, and can store 1,024 pairs of time and data pattern information.
- Detects Change of State on low to high transition or high to low transition.
- Time stamps every transition with 1 uSec resolution, and stores data and time stamp in an Input FIFO. This FIFO is 32 bits wide by 2,048 words deep and can store 682 sets of time and data pattern information.
- A PCI interrupt will be generated on the first COS, if interrupts are enabled.
- Control register is used to enable pattern generation and enable interrupts with a PCI write.
- Time can be set with a PCI write, counters are enabled with a control word write.
- One board can be designated the master and used to enable all other counters in the system. All of the counters can be clocked from the master board's clock or from their on-board 16 MHz oscillators.
- Status registers contain the following bits; Counter Enabled, Sequencer Enabled, FIFO Empty, FIFO Half Full, FIFO Full.
- PCI form factor

II. SPECIFICATIONS

Electrical Specifications

Number of Input Channels	32
Input Type	TTL
Number of Output Channels	8
Output Type	RS-232 voltage level

RS-232 Output Specifications

Output Polarity	Logic 1 = -12 Volts, Logic 0 = +12 Volts
Output Drive Current	+/- 5 mAmps (min.)
Positive Output Voltage Swing	+12V -0.3 Volts @ 5 mAmp load
Negative Output Voltage Swing	-12V +1.2 Volts @ -5 mAmp load
Output Slew Rate	15 V/uSec (typ) with 3K ohm and 51pf load

TTL Input Specifications

Input Polarity	Logic 1 = TTL High, > 2.0 Volts Logic 0 = TTL Low, < 0.8 Volts
Input Leakage Current	+/- 10 uA
Card Power Requirements	5 Volts @ 1 Amp (typ) or 3.3 Volts @ 1 Amp (typ) +12 Volts @ 5 mAmps, plus output load - 12 Volts @ 5 mAmps, plus output load

B. Environmental Specifications

Operating Temperature Range	0 to 60 degrees Celsius with forced air cooling
Storage Temperature Range	-20 to 85 degrees Celsius
Relative Humidity Range	20% to 80%, non-condensing

C. Physical Specifications

Dimensions	5.6" x 4.2"
Weight	4 oz. (typ)
I/O Connector	100-pin female, R/A, Subminiature D, 0.050", Tyco Electronics P/N 787362-9

Jumper Definitions

The PAS 2080/DIO card contains 3 jumper plugs.

Jumper PJ1 is used to select the source of the 16 MHz clock. When PJ1 is removed, the clock is supplied from the master clock input line. When PJ1 is installed, the master clock is supplied from an on board oscillator.

In systems with more than one card, one card will be designated as the master card, and it will supply the master clock signal, (MSTRCK). The master card will have PJ1 installed. All other cards in the system will be set to use the master clock input signal by removing PJ1. The card is shipped with PJ1 installed.

Jumper PJ2 is used to terminate the master clock line with a 220 / 330 ohm resistor network. In multiple card systems, the first and last cards should have the termination network enabled by installing PJ2. The master card should be located at one end of the string. The card is shipped with PJ2 installed.

Jumper PJ3 is used to configure the external clock enable line. When PJ3 is not installed, this card monitors the external clock enable input line. The line must be driven low by another card in the system, and the counter enable bit must be set in the control register, in order for the counters on this card to be enabled. When PJ3 is installed, only the counter enable bit is required to enable the counters.

When jumper PJ3 is installed, this card will drive the master enable line, (MSTREN) and all other cards in the system should be set to monitor this line. Only one card in a system should be set to drive the master enable line. The card is shipped with PJ3 installed.

TABLE 1
PLUGGABLE JUMPER DEFINITIONS

<u>Jumper #</u>	<u>Function</u>
PJ1	Master Clock Select
PJ2	Master Clock Termination
PJ3	Master Enable

Connector Definitions

A 100 pin female connector is installed through the board's front panel to provide access to the thirty-two input channels and eight output channels. The pin out of this connector is defined below.

TABLE 2
100 Pin Connector Definitions

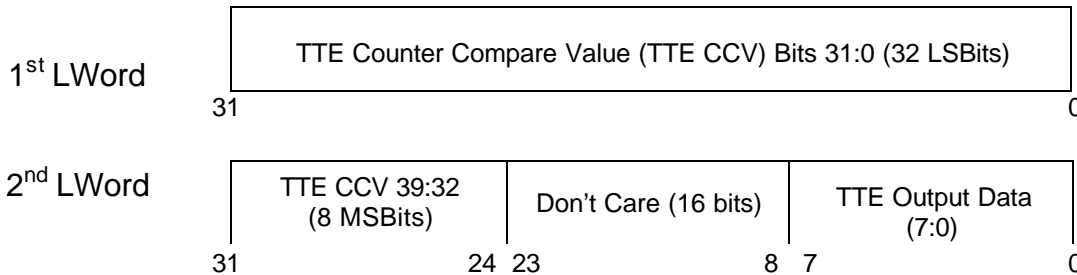
GND	100	99	+5V	GND	50	49	MREN
GND	98	97	TTE7	GND	48	47	MRCK
GND	96	95	TTE6	GND	46	45	N/C
GND	94	93	TTE5	GND	44	43	N/C
GND	92	91	TTE4	GND	42	41	N/C
GND	90	89	TTE3	GND	40	39	N/C
GND	88	87	TTE2	GND	38	37	N/C
GND	86	85	TTE1	GND	36	35	N/C
GND	84	83	TTE0	GND	34	33	N/C
GND	82	81	COS31	GND	32	31	COS15
GND	80	79	COS30	GND	30	29	COS14
GND	78	77	COS29	GND	28	27	COS13
GND	76	75	COS28	GND	26	25	COS12
GND	74	73	COS27	GND	24	23	COS11
GND	72	71	COS26	GND	22	21	COS10
GND	70	69	COS25	GND	20	19	COS9
GND	68	67	COS24	GND	18	17	COS8
GND	66	65	COS23	GND	16	15	COS7
GND	64	63	COS22	GND	14	13	COS6
GND	62	61	COS21	GND	12	11	COS5
GND	60	59	COS20	GND	10	9	COS4
GND	58	57	COS19	GND	8	7	COS3
GND	56	55	COS18	GND	6	5	COS2
GND	54	53	COS17	GND	4	3	COS1
GND	52	51	COS16	GND	2	1	COS0

III. PROGRAMMING INFORMATION

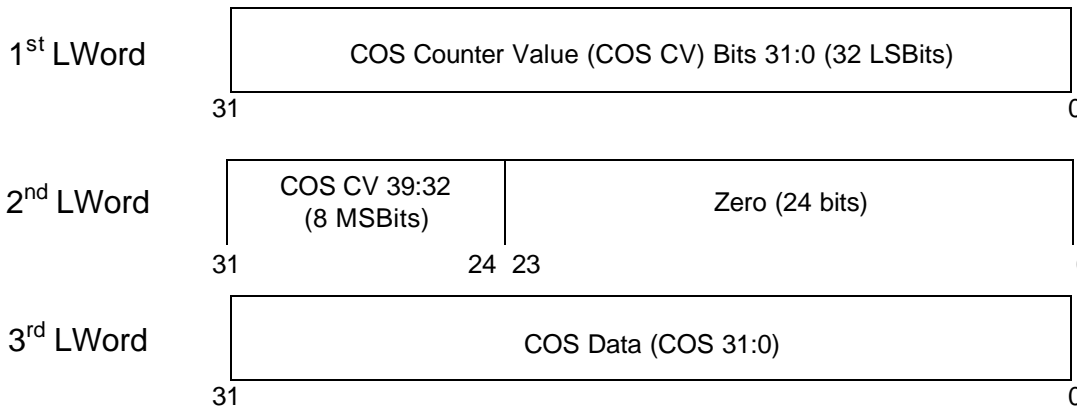
The 2080/DIO card responds to four memory-mapped long word (32 bit) locations as follows:

FIFO: Read/Write - Address Offset 0x00

Writes to address 0x00 will place the 32 bit PCI data into the TTE Output FIFO. A TTE data frame consists of two long words that define the 40-bit counter value and the 8 bit TTE data as follows:

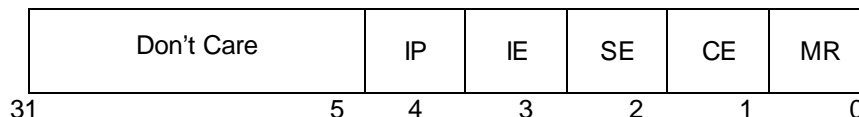


Reads from address 0x00 will place the output of the COS Input FIFO onto the PCI bus. A COS data frame consists of three long words that represent the 40 bit counter value when the COS was detected as well as the actual COS data as follows:



Control and Status Register: Read / Write: Address Offset 0x04

The Control and Status Register is located at the card's base address plus 0x04. Writes to the Control register are used to reset the card, enable the counter and sequencer, and to enable interrupts.



Bit 0 of the Control and Status register is the Master Reset bit, and steers the board reset signal. When the backplane reset occurs or following power up, all of the board's registers will get reset. Bit 0 and the board's reset line will be inactive at the end of the system reset. Writing a one to bit 0 will turn on the board reset line. When reset, the board will be disabled from detecting changes of state on the input lines, or generating output patterns. Both of the FIFOs and the 40-bit counter will be cleared when the board is reset. **In order for the card to operate normally, bit 0 must be set to a zero.** Reading bit 0 will return the value that was last written to it.

Bit 1 of the Control and Status register is the Counter Enable bit, and controls the master enable line. When this board is strapped as the master board, the master enable signal, (MSTREN), will be driven true when bit 1 is a one. In order to enable the card to monitor the inputs and generate output data patterns, both bit 1 and the master enable signal must be true. Reading bit 1 will return the value that was last written to it.

Bit 2 of the Control and Status register is the Sequencer Enable bit, and indicates the card is enabled to monitor the inputs and generate output data patterns. This bit is read only, and indicates both bit 1 AND the master enable signal are true.

Bit 3 of the Control and Status register is the Interrupt Enable bit and is used to enable interrupts when it is set to a one, and to disable interrupts when it is set to a zero. Reading bit 3 will return the value that was last written to it.

Bit 4 of the Control and Status register is the Interrupt Pending bit, and indicates that the input FIFO is not empty AND the card's interrupt logic is enabled. This signal drives an edge sensitive input into the PLX 9030 PCI controller chip. Whenever the input FIFO transitions from empty to not empty, a PCI interrupt will be generated, it interrupts are enabled.

Bits 5, 6 and 7 of the Control and Status register are not used.

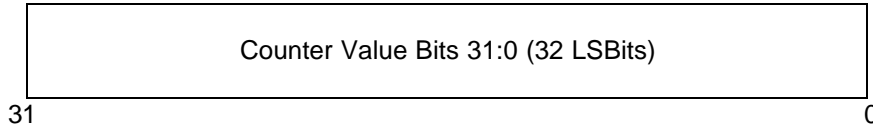
THE CONTROL REGISTER IS INITIALIZED TO ALL ZEROS ON POWER-UP

Counter Low Word: Read/Write – Address Offset 0x08

The Counter Low Word represents the low 32-bits of a 40-bit counter used to timestamp COS events and to trigger the TTE outputs. The counter contents can be written and read while it is running. However, it is possible that the counter could advance during a read operation, giving a false value. This is unlikely, but possible, so it is safest to stop the counter prior to reading its contents.

Writes to address 0x08 will place the contents of the PCI data into the low 32 bits of the counter. Reads from address 0x08 will provide the low 32 bits of the

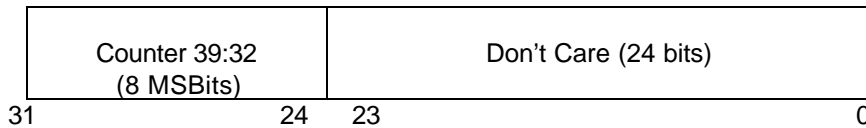
counter on the PCI data bus.



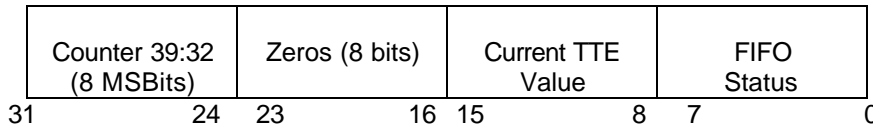
Counter High Word: Read/Write – Address Offset 0x0C

In addition to providing read/write access to the Counter High Word, reading this memory location will also provide the current state of the TTE Outputs and the FIFO Status. The counter contents can be written and read while it is running. However, it is possible that the counter could advance during a read operation, giving a false value. This is unlikely, but possible, so it is safest to stop the counter prior to reading its contents. If you only intend to read the current TTE value and FIFO status, it is unnecessary to stop the counter.

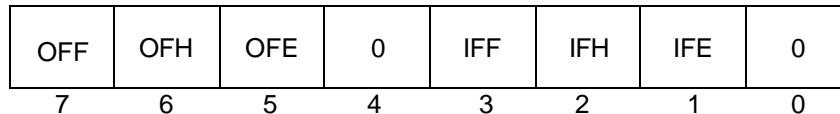
Writes are formatted as follows:



Reads are formatted as follows:



Current TTE Value – this provides the current output levels of the TTE output pins that can be used to as a diagnostic tool. FIFO Status – this provides the status of the input and output FIFO's as defined below.



- IFE = Input FIFO Empty (when '0' the COS FIFO is Empty)
- IFH = Input FIFO Half Full (when '0' the COS FIFO is Half Full)
- IFF = Input FIFO Full (when '0' the COS FIFO is Full)
- OFE = Output FIFO Empty (when '0' the TTE FIFO is Empty)
- OFH = Output FIFO Half Full (when '0' the TTE FIFO is Half Full)
- OFF = Output FIFO Full (when '0' the TTE FIFO is Full)

General Information

A 1 MHz clock is used to increment the 40-bit counter, which provides a count length of approximately 1,099,511 seconds, or 12.725 days before the counter rolls over. When the card is not enabled to generate output patterns or monitor inputs, the counter can be used as a 40-bit test register. This feature is useful for checking out the card's PCI bus interface.

In order to enable the card to monitor the input lines and generate output data patterns, the Counter Enable bit in the control register must be set to a one, AND the master enable signal must be true. When these two conditions are both true, the sequencer enable bit in the CSR will be true. This indicates the on-board sequencer logic is active to monitor the output FIFO for time matches, and to monitor the input lines for changes.

The board that is configured as the master board in the system by installing PJ3, generates the master enable signal. In single board systems, PJ3 should always be installed. In multi-board systems, one board will be configured as the master. The remaining boards will have PJ3 removed and therefore monitor the master enable signal. Pin 49 of the I/O connector is connected to the master enable signal and pin 49 of all boards in a multi-board system must be connected together. When the counter enable bit is written to the master card, it will drive the master enable signal to the remaining cards, and start all cards simultaneously. Multi-card systems also need to jumper pin 47, the master clock signal, together. Refer to the section on jumper definitions for configuring the clock jumpers.

Prior to enabling the card to generate output data patterns, the output FIFO should be loaded with a sufficient number of entries, so that the host CPU can keep up with the patterns to be generated. Data is loaded into the output FIFO as a pair of longwords. Each pair of long words contains a 40-bit time value and an 8-bit data value. When the sequencer logic is enabled, the time value from the output FIFO will be compared with the counter. Once a time match occurs the new output data will be presented to the RS-232 output drivers, and the next time value will be monitored.

When the card is enabled to monitor changes of state on the input lines, a change will generally occur as soon as the card is enabled. This is because the register that tracks the input lines is reset, when the card is disabled. If a non-zero value is present on the input lines, then the COS logic will detect a change as soon as the card is enabled. When the change is detected, the tracking register is updated to the state of the input lines, and three long words are written to the input FIFO. These three long words contain the 40-bit time value and 32 bits of input data.

The status of both FIFOs is available in the FIFO status word. The control program must monitor the status of the FIFO to make sure data is not read from an empty FIFO or written to a full FIFO.