

**Document PAS045
Revision A – 07/26/04**

**PAS 9737/AI
ENGINEERING SPECIFICATION**

**64 CHANNEL, 16 BIT
VME ANALOG INPUT CARD
Revision C – 6/30/2004**

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64 Channel 16 Bit VME Analog Input Card

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64 Channel 16 Bit VME Analog Input Card

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I. INTRODUCTION

GENERAL DESCRIPTION

The PAS 9737/AI provides 64 analog input channels multiplexed into a scanning 16-bit Analog to Digital Converter, (ADC). Low pass filters are provided for the analog input signals and four different cutoff frequencies are available as options. Digitized analog data is available to the VME bus through a dual ported RAM interface that can be read while the card continues scanning. Thirty-two bit data reads are supported, which allows two converted values to be read with a single VME transfer. VME systems with A16, A24, or A32 addressing are supported, which allows the card's base address to be located anywhere in the VME address range.

Additional features include a board identifier PROM, control and status register, and scan configuration registers.

Card Features: PAS 9737/AI

- 64 differential analog input channels
- Differential or single ended inputs jumper configurable per channel
- Optional low pass filters with corner frequencies of 10 Hz, 50 Hz, 100 Hz or 500 Hz
- Analog inputs on two ea. 78 position connectors
- 16 bit 100 KHz Analog to Digital Converter (ADC)
- Constantly scans selected channels and stores digitized results in dual port memory
- Programmable Gain Amplifier (PGA) with gains of 1 to 128 (optional)
- Input range of +/- 10.24 Volts or +/- 10.00 Volts (optional)
- Over voltage protected inputs with power on or off
- VME 6U form factor; 233 mm x 160 mm card size
- VME access: D32,D16; A32, A24, A16 Slave
- Optional VME SYSFAIL asserts on power up, jumper selectable
- Four LED's provided on the front panel; Pass, Fail, Board Access, & ADC stopped LED's
- Board Identifier PROM. (Board ID is VMEIDPAS9737AI*0) / (*) = Rev. Level
- Analog section is powered by +/- 15 Volts from an on board DC to DC converter
- Operating temperature range 0 to 60 deg. C.

II. SPECIFICATIONS

Electrical Specifications

(Un-filtered Cards)

Number of Channels	64 differential or single ended inputs
ADC input range	Bipolar +/-10.24 Volts or +/- 10.00 Volts
Resolution	16 bits
Accuracy	+/- (0.005% of reading + 0.005% FSR + 100 uV)
Temperature stability	+/- (10 PPM of reading + 7.5 PPM of FSR + 2.5 uV)/deg. C
Input bias current	40 nAmps (max.) at 0.0 Volts input
Input Impedance	5 M Ohm in parallel with 50 pF
CH.-to-CH. crosstalk	90 dB
Common mode voltage	+/- 11 Volts signal plus common mode
Common mode rejection (DC to 60 Hz, 350-ohm imbalance)	Gain = 1 90 dB (min.), 100 dB (typ.)
Over voltage protection	+/- 35 VDC sustained, power on or off
Card Power Requirements	5 Volts @ 1 Amp, (typ.)

Low Pass Filter Options*

- 0 = No filter
- 1 = 10 Hz filter
- 2 = 50 Hz filter
- 3 = 100 Hz filter
- 4 = 500 Hz filter

*Note: Low pass filters are specified at the approximate frequency where the input voltage is attenuated by 6 dB as defined by the following expression; $20 \log V(\text{out}) / V(\text{in})$. The leakage impedance of the capacitors used in the input filters forms a voltage divider with the input resistors, which results in slight variations in the gain from channel to channel. This effect is most pronounced on the 10 Hz version of the filters because they use the highest value of capacitance, thus have the highest leakage current.

Environmental Specifications

Operating Temperature Range	0 to 60 degrees C.
Storage Temperature Range	-20 to 85 degrees C.
Relative Humidity Range	20% to 80%, non-condensing

Physical Specifications

Dimensions	Form factor: Dbl (160 mm x 233 mm)
Weight	12 oz. (typ.)
Connectors	2 ea. 96 position, (VME bus connectors) 2 ea. 78 position, (Analog Input conc) 1 ea. 6 pin shrouded header (external sync. in, out and voltage ref.)

Ordering Information

The 9737/AI card is available in several different configurations that are defined by dash numbers. Each dash number has three digits defined as XYZ. Each digit defines a certain feature of the card, in this case the filter type and input voltage range. The various dash numbers are defined below.

XYZ Definitions

X = 0 (future expansion)

X0Z = No Input Filter

X1Z = 10 Hz Low Pass Input Filter

X2Z = 50 Hz Low Pass Input Filter

X3Z = 100 Hz Low Pass Input Filter

X4Z = 500 Hz Low Pass Input Filter

XY0 = +/- 10.00 Volt Full Scale Input Range, no PGA*

XY1 = +/- 10.24 Volt Full Scale Input Range, with PGA*

*PGA = Programmable Gain Amplifier

EXAMPLE: A dash number of 011 would specify a card with 10 Hz Low Pass Input Filters, a +/- 10.24 Volt Full Scale Input Range with a PGA. When ordering, the dash number follows the model number = **PAS 9737/AI-011**.

The program that is loaded into the on-board EPLD enables the PGA function. Cards without the PGA will respond as revision *A0* when their ID is read. Cards with the PGA will respond as *B0*.

Jumpers and Indicators

The 9737/AI card contains 86 jumper plugs and four LED indicators. Nineteen of the jumpers are used to set the board's VME base address, and are defined in the table 1 on page 8. When a jumper is installed, the corresponding address bit must be low to select the card's address, and when a jumper is removed, the corresponding address bit must be high. The card is shipped configured for address F0000000, so that 15 of the possible 19 address jumpers are installed.

Jumpers J1 and J2 are used to select the boards operating environment, either A16, A24 or A32, and the installation of these jumpers is defined in table 1 on page 9.

Jumper J4 allows the SYSFAIL line to be driven with bit 0 of the control register when it is installed.

Jumpers P0 through P63 are used to connect the low side of each channel to a common trace on the PCB and are available as an option. Normally the input signal wiring will take advantage of the card's differential inputs, and run separate wires from the high and low sides of the inputs back to the input signal sources. In cases where all or some of the inputs are referenced to a common ground, the jumpers can be installed to tie the low sides of the input channels together, and a single ground wire can be run to the common ground point.

TABLE 1
PLUGGABLE JUMPER DEFINITIONS

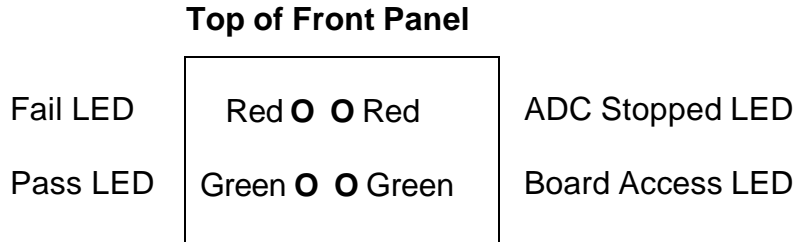
<u>Jumper #</u>	<u>Function</u>
J1	Address Space (See table below)
J2	Address Space (See table below)
J4 IN	SYSFAIL driven by control register
J13	A13
J14	A14
J15	A15
J16	A16
J17	A17
J18	A18
J19	A19
J20	A20
J21	A21
J22	A22
J23	A23
J24	A24
J25	A25
J26	A26
J27	A27
J28	A28
J29	A29
J30	A30
J31	A31

TABLE 2
Address Modifiers

J1	J2	Address Modifiers	Address Space
IN	IN	09, 0D	Extended I/O
IN	OUT	29, 2D	Short I/O
OUT	IN	39, 3D	Standard I/O
OUT	OUT	29, 2D	Short I/O

Front Panel LEDs

Four LED's arranged in a 2 by 2 array are provided at the front panel to indicate the board's status. The position of the LED's is shown below



The Fail LED powers up on, and is controlled with bit 0 of the control register. This LED can be turned off by writing a one to bit 0. The state of this LED is reflected in bit 0 of the status register. When the Fail LED is on, and J4 is installed, the SYSFAIL line will be driven on the VMEbus.

The Pass LED is controlled by bit 1 of the control register. This LED can be turned on by writing a one to bit 1, and it will power up turned off. Bit 1 in the status register reflects the state of this LED. Once the board has passed some initial power up tests this LED can be turned on to indicate successful completion of the power up sequence.

The ADC Stopped LED indicates that the ADC has not generated an end of conversion signal in the last fifteen microseconds when it is on. Since the board powers up scanning, this LED should be off. The LED will only turn on if the board if there is a failure in the scanning logic. The status of this LED is reflected in bit 2 of the status register.

The Board Access LED will turn on any time the board is accessed. A one-shot is used to drive the LED, so that it will be visible on single cycle accesses.

Connector Definitions

Two 96-position DIN connectors are installed on the backplane end of the board to make the standard VME bus connection. A pair of 78 position, high density D-sub connectors are installed through the board's front panel to provide access to the sixty-four analog input channels. The 78 position HD D-sub connectors used are made by Adam-Tech® and the part number is HDL78-SL-B. Board-to-board, crimp and poke, and solder cup mating connectors are also available from Adam-Tech®. Visit www.adam-tech.com for contact and distributor information.

A six position shrouded header is provided between the 78 position connectors to provide access to the external synchronization input and output signals. The pin definitions of these connectors provided below and on the following page.

TABLE 3

6 Position Shrouded Header, P6

Pin #	Signal Name
1	External Clock In (RFU)
2	Ground
3	External Sync In (RFU)
4	Ground
5	External Sync Out (RFU)
6	Ground

RFU = Reserved for Future Use

TABLE 4
Analog Input Connector P3
Top Connector

Pin Numbers			
CH63H	78	58	CH63L
CH62H	39	19	CH62L
CH61H	77	57	CH61L
CH60H	38	18	CH60L
CH59H	76	56	CH59L
CH58H	37	17	CH58L
CH57H	75	55	CH57L
CH56H	36	16	CH56L
CH55H	73	53	CH55L
CH54H	34	14	CH54L
CH53H	72	52	CH53L
CH52H	33	13	CH52L
CH51H	71	51	CH51L
CH50H	32	12	CH50L
CH49H	70	50	CH49L
CH48H	31	11	CH48L
CH47H	68	48	CH47L
CH46H	29	9	CH46L
CH45H	67	47	CH45L
CH44H	28	8	CH44L
CH43H	66	46	CH43L
CH42H	27	7	CH42L
CH41H	65	45	CH41L
CH40H	26	6	CH40L
CH39H	63	43	CH39L
CH38H	24	4	CH38L
CH37H	62	42	CH37L
CH36H	23	3	CH36L
CH35H	61	41	CH35L
CH34H	22	2	CH34L
CH33H	60	40	CH33L
CH32H	21	1	CH32L

TABLE 5
Analog Input Connector P4
Bottom Connector

	Pin Numbers		
CH31H	78	58	CH31L
CH30H	39	19	CH30L
CH29H	77	57	CH29L
CH28H	38	18	CH28L
CH27H	76	56	CH27L
CH26H	37	17	CH26L
CH25H	75	55	CH25L
CH24H	36	16	CH24L
CH23H	73	53	CH23L
CH22H	34	14	CH22L
CH21H	72	52	CH21L
CH20H	33	13	CH20L
CH19H	71	51	CH19L
CH18H	32	12	CH18L
CH17H	70	50	CH17L
CH16H	31	11	CH16L
CH15H	68	48	CH15L
CH14H	29	9	CH14L
CH13H	67	47	CH13L
CH12H	28	8	CH12L
CH11H	66	46	CH11L
CH10H	27	7	CH10L
CH9H	65	45	CH9L
CH8H	26	6	CH8L
CH7H	63	43	CH7L
CH6H	24	4	CH6L
CH5H	62	42	CH5L
CH4H	23	3	CH4L
CH3H	61	41	CH3L
CH2H	22	2	CH2L
CH1H	60	40	CH1L
CH0H	21	1	CH0L

III. PROGRAMMING INFORMATION

The 9737/AI card responds to word and longword reads of the sixty-four analog input channels. The card also supports word writes and reads to the control and status register, and the various scan registers, and word reads of the board identifier PROM. The card's memory map is shown below.

TABLE 6
PAS 9737/AI MEMORY MAP

BASE +0000	FF	V (56)	BASE +0001
0002	FF	M (4D)	0003
0004	FF	E (45)	0005
0006	FF	I (49)	0007
0008	FF	D (44)	0009
000A	FF	P (50)	000B
000C	FF	A (41)	000D
000E	FF	S (53)	000F
0010	FF	9 (39)	0011
0012	FF	7 (37)	0013
0014	FF	3 (33)	0015
0016	FF	7 (37)	0017
0018	FF	A (41)	0019
001A	FF	I (49)	001B
001C	FF	* (4*)	001D
001E	FF	0 (30)	001F
0020	Reserved	Reserved	0021
003E	Reserved	Reserved	003F
0040	Reserved	Control & Status	0041
0042	Reserved	ADC Scan Mode	0043
0044	Reserved	Reserved	0045
	Through	Through	
007E	Reserved	Reserved	007F
0080	CH 0	Gain	0081
	Through	Through	
00FE	CH 63	Gain	00FF
0100	Channel 0 Data		0101
0102	Channel 1 Data		0103
0104	Channel 2 Data		0105
0106	Channel 3 Data		0107
0108	Channel 4 Data		0109
010A	Channel 5 Data		010B
010C	Channel 6 Data		010D
010E	Channel 7 Data		010F
1FFE	Last Channel Data		1FFF

* = revision level

Board Identifier PROM (base + 00)

The board identifier PROM is located at an offset of 00 (hex) from the base address, and can be read with word reads only. The least significant byte of the word will contain valid data, and the most significant byte will contain FF. The ID PROM contains 16 ASCII characters that specify the board's model number and revision level. A write to the ID PROM will handshake, but not transfer any data.

TABLE 7

Control and Status Register (base + 41)

7	6	5	4	3	2	1	0
Loop Back	Loop Back	Loop Back	SW Reset Pulse	Loop Back	ADC Stop	Pass LED	Fail LED

Bits 7-5 Loopback. These bits will return the values last written to them.

Bit 4 Writing a 1 to this bit will generate a software-reset pulse. The software reset stops the conversion in process. It also resets the scan mode register, and disables scanning. This bit will always return a 0 when read.

Bit 3 Loopback. This bit will return the value that was last written to it.

Bit 2 This bit indicates that a conversion has not occurred in the last 15 uSec. Writing this bit has no effect.

1 = ADC has not performed a conversion in the last 15 uSec.

0 = ADC has performed a conversion in the last 15 uSec

Bit 1 This bit controls the Pass LED

1 = Turn on the Pass LED

0 = Turn off the Pass LED

Bit 0 This bit controls the Fail LED. The SYSFAIL line will also be asserted when the Fail LED is on.

1 = Turn off the Fail LED

0 = Turn on the Fail LED

ADC Scan Mode Register (base + 43)

This 8-bit register determines the scanning mode for the analog inputs used on this board. The bits are defined below:

TABLE 8
ADC Scan Mode Register

7	6	5	4	3	2	1	0
Enable Scan	Cont Scan	Gain Init	Scan Mode	Scan Mode	Scan Mode	Scan Mode	Scan Mode
			4	3	2	1	0

Bit 7 This bit is used to enable or disable scanning of the analog input channels. The enable scan bit is cleared on power up, SYSRST or software reset.

- 0 = Scanning Disabled
- 1 = Scanning Enabled

Bit 6 This bit enables or disables continuous scanning of the analog input channels. When continuous scanning is enabled the scan sequencer will start the scan sequence over once the last channel has been sampled. The continuous scan bit is cleared on power up, SYSRST or software reset.

- 0 = Continuous scanning disabled
- 1 = Continuous scanning enabled

Bit 5 This bit is used to enable the sequencer to use channel gain values that are stored in memory. When the gain initialized bit is clear the sequencer will scan all of the channels at unity gain. The gain-initialized bit is cleared on power up, SYSRST or software reset. This bit is only functional on cards with the PGA option (XY1).

- 0 = Sample all channels at unity gain
- 1 = Sample each channel at the gain specified by the Channel Gain Memory

Bits 4-3 Loopback. These bits will return the last value written to them.

Bits 2-0 These bits are used to determine how many time the sequencer will scan the sixty-four input channels before it either stops or repeats the scan. The bits are defined in table 9 on the following page.

TABLE 9
Scan Mode Bits

SM2	SM1	SM0	Blocks Scanned	Stop Address
0	0	0	1	017F
0	0	1	1	017F
0	1	0	2	01FF
0	1	1	4	02FF
1	0	0	8	04FF
1	0	1	16	08FF
1	1	0	32	10FF
1	1	1	62	1FFF

TABLE 10
Channel Gain Memory (base + 80 - FF)

7	6	5	4	3	2	1	0
					Gain 2	Gain 1	Gain 0

The Channel Gain Memory is used to specify the gain that each channel will use when sampling and converting input signals. This information must be programmed before the card begins sampling data. Memory location 81 contains the gain for channel 0 and the gain information for subsequent channels is contained in the ascending odd memory locations. The gain value for channel 63 is contained at location FF. Gain can be programmed in binary steps from 1 to 128, and the gain codes are shown below. The gain values can be read back over the VME bus when the card is not scanning input channels. When the card is scanning the gain values are only available to the scan sequencer. The gain memory is only available on cards with the PGA option (XY1).

TABLE 11
Gain Codes

Gain 2	Gain 1	Gain 0	Gain Value	Full Scale Range
0	0	0	1	+/- 10.24 V
0	0	1	2	+/- 5.12 V
0	1	0	4	+/- 2.56 V
0	1	1	8	+/- 1.28 V
1	0	0	16	+/- 640 mV
1	0	1	32	+/- 320 mV
1	1	0	64	+/- 160 mV
1	1	1	128	+/- 80 mV

Channel Data Memory (100 – 1FFF)

The Channel Data Memory is used to store the converted values from the scanned channels. Data is stored in 16 bit, 2's complement format. The first value in a data scan will be stored at location 100 and the sequencer can fill the entire RAM array up to address 1FFF. When scanning is disabled, the VME bus can write to the Channel Data Memory. This allows the memory to be filled with test patterns and then read back to verify the functionality of the memory and the data busses. When the card is scanning, writes from the VME bus are disabled, and only the scan sequencer can write to the Channel Data Memory.

The card can be programmed to use as little as 64 words of Channel Data Memory, or up to 3968 words. When the card is programmed to fill blocks of data with 64 channels per block, the second block will start at location 180(hex).

Once a scan is complete, the card can be programmed to automatically start the scan over, or to stop the scan sequencer. A convenient way to use this card is to set the card to scan all of the channels, and then repeat the scan cycle. Whenever a data value is required, the program can read the desired memory location and get the latest digitized analog value. In this mode of operation, the card's response time similar to a digital input card.

IV. CALIBRATION PROCEDURE for +/- 10.24V Card with PGA

Install the PAS 9737/AI card in a VME chassis, and allow the card to stabilize for approximately five minutes. A test program is required that will read and display the values of all channels on the card.

ADC Zero Adjustment (R26)

Connect a precision voltage standard to the input of channel zero, with the high side of the voltage standard connected to the low side of the channel, (P4I-1) and the low side of the voltage standard connected to the high side of the channel, (P4I-2). Connect the low side of the channel to earth ground, and select 0.0000 Volts out of the voltage standard. Adjust R26 for a reading of 0000 (hex) on channel zero.

ADC Gain Adjustment (R28)

Leave the voltage standard configured as in the previous step, and select -10.2375 Volts out of the standard. Adjust R28 for a reading of 7FF8 (hex). Select +10.2375 Volts out of the voltage standard, and verify a reading of 8008 (hex).

Common Mode Adjustment (R36)

Reverse the leads from the voltage standard to the card. The high side of the voltage standard is connected to the high side of the channel (P4I-2), and the low side of the voltage standard is connected to the low side of the channel (P4I-1). Select +10.2375 Volts out of the standard and adjust R36 for a reading of 7FF8 (hex). Select -10.2375 Volts out of the standard, and verify a reading of 8008 (hex).

PGA Zero Adjustment (R37)

Set up the test program to scan all of the even channels at a gain of one, and all of the odd channels at a gain of 32. Short the inputs of all channels together, and connect all inputs to the card's analog ground. Adjust R37 so that all channels display the same digital value. Adjust R26 until all channels read zero counts. Verify all previous calibrations, and repeat any adjustments as necessary.

All Inputs Functional Test

Set up the test program to scan all channels at a gain of one. Input +10.2375 Volts, 0.0000 Volts and -10.2375 Volts on each channel, one channel at a time, and verify the proper digital value.

V. CALIBRATION PROCEDURE for +/- 10.00V Card w/out PGA

Install the PAS 9737/AI card in a VME chassis, and allow the card to stabilize for approximately five minutes. A test program is required that will read and display the values of all channels on the card.

ADC Zero Adjustment (R26)

Connect a precision voltage standard to the input of channel zero, with the high side of the voltage standard connected to the low side of the channel, (P4I-1) and the low side of the voltage standard connected to the high side of the channel, (P4I-2). Connect the low side of the channel to earth ground, and select 0.0000 Volts out of the voltage standard. Adjust R26 for a reading of 0000 (hex) on channel zero.

ADC Gain Adjustment (R28)

Leave the voltage standard configured as in the previous step, and select -9.9976 Volts out of the standard. Adjust R28 for a reading of 7FF8 (hex). Select +9.9976 Volts out of the voltage standard, and verify a reading of 8008 (hex).

Common Mode Adjustment (R36)

Reverse the leads from the voltage standard to the card. The high side of the voltage standard is connected to the high side of the channel (P4I-2), and the low side of the voltage standard is connected to the low side of the channel (P4I-1). Select +9.9976 Volts out of the standard and adjust R36 for a reading of 7FF8 (hex). Select -9.9976 Volts out of the standard, and verify a reading of 8008 (hex).

All Inputs Functional Test

Set up the test program to scan all channels at a gain of one. Input +9.9976 Volts, 0.0000 Volts and -9.9976 Volts on each channel, one channel at a time, and verify the proper digital value.