
**PAS 9739/AI
ENGINEERING SPECIFICATION**

**39 CHANNEL PHOTODIODE
AND DUAL ADC CARD
VME ANALOG INPUT CARD
Revision A (12/14/2000)**

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39 Channel Photodiode and Dual ADC Card VME Analog Input Card

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I. INTRODUCTION

GENERAL DESCRIPTION

The PAS 9739/AI is a VME based, thirty-nine channel, photodetector and dual ADC, Analog Input Card. Each channel consists of a photodiode driving the inputs of a pair of current to voltage conversion amplifiers. The amplifiers have different gains and provide high and low sensitivity outputs. The amplified outputs are digitized by a pair of twelve bit, 500 KHz, Analog to Digital Converters (ADCs) and stored in a memory array that is accessible by the VME bus.

Each ADC chip consists of two, 500KHz, twelve bit ADCs with a three channel multiplexer connected to the input of each ADC. In normal operation, the card simultaneously samples and converts the high and low sensitivity signals associated with a given photodetector, and stores the digitized data in the memory array. After completion of the conversion, the card increments to the next channel and performs a pair of conversions. This repeats continuously for the three channels connected to each ADC.

Thirteen ADC chips are provided on this card, and they synchronously scan their three input channels. The converted data is stored in an array that is accessible by the VME bus while the card is scanning. Data from the high and low sensitivity channels can be read with a single 32 bit VME transfer. This approach provides data for all channels with a maximum latency of six microseconds plus the VME bus access time.

Calibration circuitry is provided that will inject known currents into the front-end amplifiers, when enabled with a control instruction. The calibration feature is useful for verifying the functionality of the input amplifiers and A to D converters.

The card format is 9U by 340mm and it is configured to work in a special chassis that hardwires address bits eight through fifteen in the backplane. VME systems with A16, A24, and A32 addressing are also supported, and jumper plugs are provided to set the card's address, and width of the address bus. Data bus widths of 16 and 32 bits are supported, and the instruction selects the transfer type. A board identifier PROM, serial number register, test registers, and a control and status register are also provided.

Card Features: PAS 9739/AI

- Thirty-nine channel, photo detector and dual gain analog input card
- Dual gain amplifiers provide high and low sensitivity outputs for each photodiode
- Thirteen synchronously scanning ADC chips
- Each ADC chip contains two, twelve bit, 500 KHz Analog to Digital Converters and two, three to one multiplexers
- High and low sensitivity outputs of each channel are converted simultaneously
- High and low sensitivity data is available in a single 32 bit VME read
- Maximum data latency is six microseconds plus VME transfer time
- Calibration signals are provided on every channel
- Thirty-two bit test register provided to verify the VME bus
- Unique sixteen bit serial number on each board that can be read over the VME bus
- Eurocard 9U x 340 mm form factor
- VME access: D32, D16; A32, A24, A16
- Four LED on the front panel provide the following status; Pass, Fail, Calibration in Process, Board Access
- Jumper enables VME SYSFAIL to assert on power up
- No VME interrupts
- Board identifier PROM; ID code is VMEIDPAS9739AIA0
- Operating temperature range 0 to 55 deg. Celsius, with forced air cooling

II. SPECIFICATIONS

Electrical Specifications

Number of Channels	39
Resolution	12 bits
Input Voltage Range of ADC	0 to 5 Volts
LSB bit weight	1.22 mVolt
Conversion Time	1.75 uSec (typ.)
Acquisition Time	0.25 uSec (typ.)
Throughput Rate	500 KHz (min.)
Integral Linearity	+/- 0.5 LSB (typ), +/- 1 LSB (max.)
Differential Linearity	+/- 0.4 LSB (typ)
High Sensitivity Gain	10 V/uA
Low Sensitivity Gain	100 mV/uA
High Sensitivity Calibration Current	0.2 uA
Low Sensitivity Calibration Current	5.0 uA
High Sensitivity Converted Calibration Voltage	2.0 Volts
Low Sensitivity Converted Calibration Voltage	0.5 Volts
Photo detector Dark Current	1 nA (typ.), 5 nA (max.)
Photo detector Responsivity	
Type 1	0.75 A/W (min.), 0.85 A/W (typ.)
Type 2	0.85 A/W (min.), 0.92 A/W (typ.)
Type 3	0.90 A/W (min.), 0.95 A/W (typ.)
Card Power Requirements	5 Volts @ TBD Amps (typ), TBD Amps (max.) + 12 Volts @ TBD Amps (typ.) - 12 Volts @ TBD Amps (typ.)

Environmental Specifications

Operating Temperature Range	0 to 55 degrees C with forced air cooling.
Storage Temperature Range	-20 to 85 degrees C.
Relative Humidity Range	20% to 80%, non-condensing

Physical Specifications

Dimensions	Form factor: 9U x 340 mm
Weight	TBD oz. (typ)
Connectors	2 ea. 96 pos. DIN (VME bus)

Jumpers and Indicators

The 9739/AI card contains 27 jumper plugs and four LED indicators. The first 24 jumpers set the board's VME base address, and are defined in the table 1. When a jumper is installed, the corresponding address bit must be low to select the card's address, and when a jumper is removed the corresponding address bit must be high. The card is shipped with none of the jumpers installed, since it will normally be used in a chassis that has the address hard wired in the P2 backplane connector. The P2 pin numbers for given address bits are also defined in table 1.

Jumpers J25 and J26 are used to select the boards operating environment, either A16, A24 or A32, and the installation of these jumpers is defined in table 1. Boards are shipped with neither of these jumpers installed since they will normally be used in A16 environments.

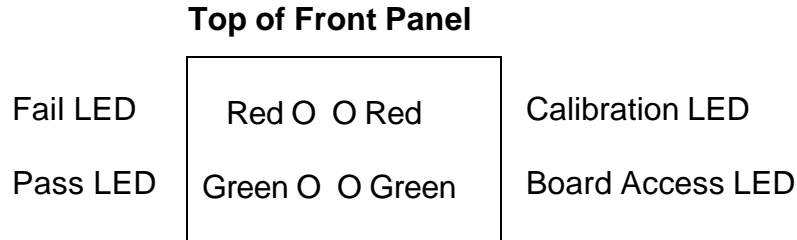
Jumper J28 allows the SYSFAIL line in the VME bus to be driven with bit 0 of the control register when it is installed. This jumper is installed for shipping.

TABLE 1
JUMPER PLUG DEFINITIONS

<u>Jumper #</u>	<u>Function</u>	<u>P2 #</u>
J1	A8	a1
J2	A9	a2
J3	A10	a3
J4	A11	a4
J5	A12	a5
J6	A13	a6
J7	A14	a7
J8	A15	a8
J9	A16	
J10	A17	
J11	A18	
J12	A19	
J13	A20	
J14	A21	
J15	A22	
J16	A23	
J17	A24	
J18	A25	
J19	A26	
J20	A27	
J21	A28	
J22	A29	
J23	A30	
J24	A31	
J25 IN, J26 IN	A32 Addressing	
J25 IN, J26 OUT	A24 Addressing	
J25 OUT, J26 X	A16 Addressing	
J28 IN	SYSFAIL controlled by CSR	

Front Panel LEDs

Four LED's arranged in a 2 by 2 array are provided at the front panel to indicate the board's status. The position of the LED's is shown below



The Fail LED powers up on, and is controlled with bit 0 of the control register. Writing a one to bit 0 can turn off this LED. The state of this LED is reflected in bit 0 of the status register. When the Fail LED is on, and J28 is installed, the SYSFAIL line will be driven on the VMEbus.

The Pass LED is controlled by bit 1 of the control register. This LED can be turned on by writing a one to bit 1, and it will power up turned off. Bit 1 in the status register reflects the state of this LED. Once the board has passed some initial power up tests this LED can turned on to indicate successful completion of the power up sequence.

The Calibration LED is controlled by bit 2 of the control register. This LED can be turned on by writing a one to bit 1, and it will power up turned off. Bit 2 in the status register reflects the state of this LED. When bit 2 in the control register is set to one, the calibration current signals will be connected to the input of the photo detector amplifiers.

The Board Access LED will turn on any time the board is accessed. A one-shot is used to drive the LED, so that it will be visible on single cycle accesses.

III. PROGRAMMING INFORMATION

The memory map of the 9739/AI card is shown below. The card responds to word reads of the board identifier PROM and Serial Number Register, (SNR). Word writes and reads to the Control and Status Register, (CSR), are supported. A thirty two-bit test register is available to verify the operation of the VME bus, and this register responds to word and long word reads and writes. Word and longword reads of the thirteen Analog to Digital Converters, (ADC's), are supported. This allows two ADC values to be read with a single VME bus transfer. More detailed information on these registers is provided following the memory map.

TABLE 2
PAS 9739/AI MEMORY MAP

00,01	Channel 0 High Sensitivity
02,03	Channel 0 Low Sensitivity
04,05	Channel 1 High Sensitivity
06,07	Channel 1 Low Sensitivity
08,09	Channel 2 High Sensitivity
0A,0B	Channel 2 Low Sensitivity
0C,0D	Reserved
0E,0F	Reserved
10,11	Channel 3 High Sensitivity
12,13	Channel 3 Low Sensitivity
14,15	Channel 4 High Sensitivity
16,17	Channel 4 Low Sensitivity
18,19	Channel 5 High Sensitivity
1A,1B	Channel 5 Low Sensitivity
1C,1D	Reserved
1E,1F	Reserved
20,21	Channel 6 High Sensitivity
22,23	Channel 6 Low Sensitivity
24,25	Channel 7 High Sensitivity
26,27	Channel 7 Low Sensitivity
28,29	Channel 8 High Sensitivity
2A,2B	Channel 8 Low Sensitivity
2C,2D	Reserved
2E,2F	Reserved
30,31	Channel 9 High Sensitivity
32,33	Channel 9 Low Sensitivity
34,35	Channel 10 High Sensitivity
36,37	Channel 10 Low Sensitivity
38,39	Channel 11 High Sensitivity
3A,3B	Channel 11 Low Sensitivity
3C,3D	Reserved

TABLE 2
PAS 9739/AI MEMORY MAP

3E,3F	Reserved
40,41	Channel 12 High Sensitivity
42,43	Channel 12 Low Sensitivity
44,45	Channel 13 High Sensitivity
46,47	Channel 13 Low Sensitivity
48,49	Channel 14 High Sensitivity
4A,4B	Channel 14 Low Sensitivity
4C,4D	Reserved
4E,4F	Reserved
50,51	Channel 15 High Sensitivity
52,53	Channel 15 Low Sensitivity
54,55	Channel 16 High Sensitivity
56,57	Channel 16 Low Sensitivity
58,59	Channel 17 High Sensitivity
5A,5B	Channel 17 Low Sensitivity
5C,5D	Reserved
5E,5F	Reserved
60,61	Channel 18 High Sensitivity
62,63	Channel 18 Low Sensitivity
64,65	Channel 19 High Sensitivity
66,67	Channel 19 Low Sensitivity
68,69	Channel 20 High Sensitivity
6A,6B	Channel 20 Low Sensitivity
6C,6D	Reserved
6E,6F	Reserved
70,71	Channel 21 High Sensitivity
72,73	Channel 21 Low Sensitivity
74,75	Channel 22 High Sensitivity
76,77	Channel 22 Low Sensitivity
78,79	Channel 23 High Sensitivity
7A,7B	Channel 23 Low Sensitivity
7C,7D	Reserved
7E,7A	Reserved
80,81	Channel 24 High Sensitivity
82,83	Channel 24 Low Sensitivity
84,85	Channel 25 High Sensitivity
86,87	Channel 25 Low Sensitivity
88,89	Channel 26 High Sensitivity
8A,8B	Channel 26 Low Sensitivity
8C,8D	Reserved
8E,8F	Reserved
90,91	Channel 27 High Sensitivity

TABLE 2
PAS 9739/AI MEMORY MAP

92,93	Channel 27 Low Sensitivity
94,95	Channel 28 High Sensitivity
96,97	Channel 28 Low Sensitivity
98,99	Channel 29 High Sensitivity
9A,9B	Channel 29 Low Sensitivity
9C,9D	Reserved
9E,9F	Reserved
A0,A1	Channel 30 High Sensitivity
A2,A3	Channel 30 Low Sensitivity
A4,A5	Channel 31 High Sensitivity
A6,A7	Channel 31 Low Sensitivity
A8,A9	Channel 32 High Sensitivity
AA,AB	Channel 32 Low Sensitivity
AC,AD	Reserved
AE,AF	Reserved
B0,B1	Channel 33 High Sensitivity
B2,B3	Channel 33 Low Sensitivity
B4,B5	Channel 34 High Sensitivity
B6,B7	Channel 34 Low Sensitivity
B8,B9	Channel 35 High Sensitivity
BA,BB	Channel 35 Low Sensitivity
BC,BD	Reserved
BE,BF	Reserved
C0,C1	Channel 36 High Sensitivity
C2,C3	Channel 36 Low Sensitivity
C4,C5	Channel 37 High Sensitivity
C6,C7	Channel 37 Low Sensitivity
C8,C9	Channel 38 High Sensitivity
CA,CB	Channel 38 Low Sensitivity
CC,CD	Reserved
CE,CF	Reserved
D0,D1	Reserved, ID PROM V (56)
D2,D3	Reserved, ID PROM M (4D)
D4,D5	Reserved, ID PROM E (45)
D6,D7	Reserved, ID PROM I (49)
D8,D9	Reserved, ID PROM D (44)
DA,DB	Reserved, ID PROM P (50)
DC,DD	Reserved, ID PROM A (41)
DE,DF	Reserved, ID PROM S (53)
E0,E1	Reserved, ID PROM 9 (39)
E2,E3	Reserved, ID PROM 7 (37)
E4,E5	Reserved, ID PROM 3 (33)

TABLE 2
PAS 9739/AI MEMORY MAP

E6,E7	Reserved, ID PROM 9 (39)
E8,E9	Reserved, ID PROM A (41)
EA,EB	Reserved, ID PROM I (49)
EC,ED	Reserved, ID PROM A (41)
EE,EF	Reserved, ID PROM 0 (30)
F0,F1	Reserved, Control and Status Register
F2,F3	Serial Number Register
F4,F5	Test Register
F6,F7	Test Register
F8,F9	Reserved
FA,FB	Reserved
FC,FD	Reserved
FE,FF	Reserved

Analog to Digital Converters

The ADCs can be read starting at the card's base address, with either word or longword transfers. Refer to the card's memory map for the location of each ADC. The data returned by the ADC's is sixteen bits wide. Bit 15 is a one if the output word contains valid data. Bits fourteen through twelve store channel information as indicated in the table below. The twelve bit output data is stored from bit 11 (MSB) to bit 0 (LSB). Two ADC outputs can be read with a single 32-bit VME bus read. This allows the high and low sensitivity values for a given channel to be obtained with a single instruction. If an ADC address is written, the card will handshake with the VME bus, but will not write any data.

TABLE 3

15	14	13	12	11	10	1 0	1	0
Valid Data	Chan 2	Chan 1	Chan 0	Data 11	Data 10	Data 9-2	Data 1	Data 0

TABLE 4

Data Channel	Bit 14 Chan 2	Bit 13 Chan 1	Bit 12 Chan 0
A High Sensitivity	0	0	0
A Low Sensitivity	0	0	1
B High Sensitivity	0	1	0
B Low Sensitivity	0	1	1
C High Sensitivity	1	0	0
C Low Sensitivity	1	0	1

Board Identifier PROM

The board identifier PROM is located starting at the card's base address plus D0 (hex), and can be read with word reads only. Only the least significant byte of the word will contain valid data, and the most significant byte will contain FF. The ID PROM contains 16 ASCII characters that specify the board's model number and revision level. A write to the ID PROM location will handshake, but not transfer any data.

Control and Status Register

The Control & Status Register, (CSR), is located at the card's base address plus F1 (hex) and is used to control the front panel LED's, calibration signals and generate a software reset. The format of this register is shown below.

TABLE 5

Control & Status Register

7	6	5	4	3	2	1	0
Loop Back	Loop Back	Loop Back	Loop Back	Soft Reset	Cal Enable	Pass LED	Fail LED

Bit 0 of the CSR steers the Fail LED at the front panel. The SYSFAIL line on the VME backplane, will also be asserted if J28 is installed, and bit 0 is reset in either CSR. When the card is reset the Fail LED will come on. Writing a one to bit 0 can turn off the LED and the SYSFAIL line. Reading bit 0 returns the state that was last written.

Bit 1 of the CSR controls the Pass LED. This LED will be turned off when the board is reset or when a zero is written to bit 1. Writing a one to bit 1 can turn on the LED. Reading bit 1 returns the state that was last written.

Bit 2 of the CSR controls the calibration circuitry and LED. The Calibration LED and circuit will be turned off when the board is reset or when a zero is written to bit 1. Writing a one to bit 2 can turn on the Calibration circuitry and LED. When calibration is enabled, a 0.2 micro-amp current will be injected into the high sensitivity amplifier, and a 5.0 micro-amp current will be injected into the low sensitivity amplifier. Reading bit 2 returns the state that was last written.

Writing to bit 3 of the CSR will generate a software-reset pulse. Following a software reset, the Fail LED will be on, the Pass LED will be off and calibration will be disabled. This bit will always return a 0 when read.

Bits 4 through 7 of the CSR are loopback bits, and return the value that was last written. These bits are cleared to zero following a system or software reset.

Serial Number Register

The Serial Number Register is a read only register located at the card's base address plus F2 (hex). Each card is assigned a unique serial number by installing jumpers. Reading this location will return the sixteen-bit value of the serial number. Writes to the SNR address will handshake with the VME bus, but no data will be transferred.

Test Register

The 32-bit Test Register is located at an offset of F4 (hex) from the base address. This register can be written to with either words or longwords, and read back with either words or longwords. Reading the test register returns the last value written to it. This is useful for testing the card's internal data busses, and VME bus interface.