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PAS 9740/DO
ENGINEERING SPECIFICATION

16 CHANNEL PATTERN GENERATOR
WITH 1 uSEC RESOLUTION
VME DIGITAL OUTPUT CARD
Revision E (09/17/2003)

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16 Channel Pattern Generator with 1 uSec Resolution VME Digital Output Card

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Receiver Gate Generator
VME Digital Output Card

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I. INTRODUCTION

GENERAL DESCRIPTION

The PAS 9740/DO is a VME based, 16 channel, and pattern generator with 1 uSec resolution. Time and output data values that represent the pattern to be generated are loaded from the VME bus into an onboard FIFO. The card contains a 32 bit, 1 MHz counter that can be set and enabled by the VME bus. When the card is enabled to generate output data patterns, the first time value in the FIFO will be monitored until it matches the value of the 32-bit counter. When the match occurs, the output data pattern will be presented to the card's output drivers, and the next time value in the FIFO will be compared to the value of the counter. The FIFO is 512 words deep by 32 bits wide, and stores 32 bit time values followed by 16 bit data values. This allows 256 time and data value pairs to be stored in the FIFO at any given time.

VME systems with A16, A24, or A32 addressing, and data bus widths of 16 and 32 bits are supported. Jumper plugs are used to configure the width of the address and data buses. The output signals are RS-232 voltage levels on the PAS 9740/DO-000, and TTL levels on the PAS 9740/DO-001 version. A DB37 female connector mounted through the front panel provides access to the output signals. A board identifier PROM, control register and status register are provided in addition to the 32 bit 1 uSec counter and 512 by 32 FIFO.

Card Features: PAS 9740/DO

- 16, RS- 232 voltage level (-000 version) or TTL output channels (-001 version).
- Output signals on DB37 female connector at the front panel.
- On board FIFO stores output data pattern and time stamp. This FIFO is 32 bits wide by 512 words deep, and can store 256 sets of time and data pattern information.
- VME bus can write 16-bit data value to the FIFO with a 16 or 32 bit transfer.
- VME bus can write 32-bit time value to the FIFO or counter with a 32-bit transfer or 2, 16 bit transfers.
- Control register is used to enable pattern generation and enable output drivers with a VME write.
- One board can be designated the master and used to enable all other counters in the system. All of the counters can be clocked from the VME system clock or from their on board 16 MHz oscillators.
- Status register contains the following bits; Pass, Fail, Counter Enabled, Sequencer Enabled, Output Drivers Enabled, FIFO Empty, FIFO Half Full, and FIFO Full.
- VME 6U form factor; 233 mm x 160 mm card size.
- VME access: D32, D16; A32, A24, A16 Slave. No VME interrupts.
- Optional VME SYSFAIL assert on power up, SYSFAIL LED and Board Access LED on front panel.
- Board identifier PROM; ID code is VMEID PAS9740DO **. (** Is revision level)

II. SPECIFICATIONS

Electrical Specifications

Number of Channels	16
Output Type	RS-232 voltage level, with output enable/disable or TTL voltage level
Oscillator Frequency	16.000 MHz
Frequency Stability Inclusive of 25^{o}C tolerance & operating temperature range	+/- 20ppm

RS-232 Output Specifications (-000 version)

Output Polarity	Logic 1 = -12 Volts, Logic 0 = +12 Volts
Output Drive Current	+/- 5 mAmps (min.)
Positive Output Voltage Swing	+12V -0. 3 Volts @ 5 mAmp load
Negative Output Voltage Swing	-12V +1.2 Volts @ -5 mAmp load
Output Slew Rate load	15 V/uSec (typ) with 3 Kohm and 51-pf
Output Enable	Programmable

TTL Output Specifications (-001 version)

Output Polarity	Logic 1 = TTL high, Logic 0 = TTL low
Output Driver	74ALS273
High Level Output Voltage	2.4 V (min.), 3.2 V (typ.) @ -2.6 mA
Low Level Output Voltage	0.35 V (typ.), 0.5 V (max.) @ 24 mA
Prop time clock to output	
Low to high transition	2 ns (typ.), 12 ns (max.)
High to low transition	3 ns (typ.), 15 ns (max.)
Output Enable	Always enabled
Card Power Requirements	5 Volts @ 2 Amps (typ) +12 Volts @ 5 mAmps, plus output load -12 Volts @ 5 mAmps, plus output load

Environmental Specifications

Operating Temperature Range cooling	0 to 60 degrees Celsius with forced air-
Storage Temperature Range	-20 to 85 degrees C
Relative Humidity Range	20% to 80%, non-condensing

Physical Specifications

Dimensions	Form factor: Double (160 mm x 233 mm)
Weight	16 oz. (typ)
Connectors	2 ea. 96 pos. DIN (VME bus connectors) 1 ea. DB37 female (output data connector)

Ordering Information

The PAS 9740/DO card is available in two different configurations that are defined by three digit dash numbers. These dash numbers are defined below:

PAS 9740/DO-000 = RS-232 Level Output Signals

PAS 9740/DO-001 = TTL Level Output Signals

Jumpers and Indicators

The 9740/DO card contains 31 jumper plugs and two LED indicators. The first 24 jumpers are used to set the board's VME base address, and are defined in table 1 on page 9. When a jumper is installed, the corresponding address bit must be low to select the card's address, and when a jumper is removed the corresponding address bit must be high. The card is shipped configured for address F0000000, so that 20 of the possible 24 address jumpers are installed.

Jumpers J25 and J26 are used to select the boards operating environment, either A16, A24 or A32, and the installation of these jumpers is defined in table 1.

Jumper J27 is used to set the function of the Pass/Access LED. When it is installed in position 1-2, the LED is controlled by bit 1 in the control register. When J27 is in position 2-3 the LED indicates the board is being accessed.

Jumper J28 allows the SYSFAIL line to be driven with bit 0 of the control register when it is installed.

Jumper J29 is used to select the source of the 16 MHz clock. When J29 is in position 1-2 the clock is supplied from the VME SYSCLK line. When J29 is in position 2-3 the clock is supplied from an on-board oscillator.

Jumpers J30 and J31 are used to configure the external clock enable line. In order to enable the card to generate patterns, the external enable signal must be true, AND the counter enable bit, (Bit 4) in the control register must be set to a one. This enables the on-board sequencer logic and sets the sequencer enable bit in the status register.

Installing J30 causes the external enable, (EXTENL), signal to be driven out on pin 1 of P3, whenever bit 4 in the control register is set to a one. In multiple board systems, this jumper must always be installed on the master board. All boards that are not masters must have J30 removed, in order to monitor the EXTENL signal. This signal must also be bussed together on all boards in the system. In single board systems, J30 should be installed, so that the sequencer enable bit sets, as soon as the counter enable bit is set in the control register.

Installing J31 will cause the external enable line to always be true. In single board systems, this will cause the sequencer to be enabled as soon as the counter enable bit is set in the control register. The recommended configuration for single board systems is to install J30 and remove J31.

TABLE 1

JUMPER PLUG DEFINITIONS

Jumper #	Function
J1	A8
J2	A9
J3	A10
J4	A11
J5	A12
J6	A13
J7	A14
J8	A15
J9	A16
J10	A17
J11	A18
J12	A19
J13	A20
J14	A21
J15	A22
J16	A23
J17	A24
J18	A25
J19	A26
J20	A27
J21	A28
J22	A29
J23	A30
J24	A31
J25 IN, J26 IN	A32 Addressing
J25 IN, J26 OUT	A24 Addressing
J25 OUT, J26 X	A16 Addressing
J27 (1-2)	LED 2 indicates board passed
J27 (2-3)	LED 2 indicates board accessed
J28 IN	SYSFAIL controlled by control register
J29	16 MHz Clock Source
J30, 31	External clock enable

Two LED’s are provided at the front panel to indicate the board's status. The upper LED, (LED 1) is the Fail LED, and powers up on. This LED is controlled with bit 0 of the control register, and can be turned off by writing a one to that bit. The SYSFAIL line will also be driven when Fail LED is on, if J28 is installed.

The lower LED, (LED 2), is the Pass/Access LED, and its function is selected with J27. When it is configured for the pass function, it is controlled by bit 1 of the control register. LED 2 can be turned on by writing a one to bit 1, and it will power up turned off. This LED can be used to indicate the board has passed some initial power up tests when it is configured for the pass function. When configured for the access function, LED 2 will turn on any time the board is accessed. A one-shot is used to drive this LED, so that it will be visible on single cycle accesses.

Connector Definitions

Two 96 position DIN connectors are installed on the backplane end of the board to make the standard VME bus connection. A DB37 female connector is installed through the board's front panel to provide access to the sixteen output channels. The pin out of this connector is defined on the following page.

TABLE 2

DB37 Connector

		19	OUTPUT 1
GND	37		
		18	OUTPUT 2
GND	36		
		17	OUTPUT 3
GND	35		
		16	OUTPUT 4
GND	34		
		15	OUTPUT 5
GND	33		
		14	OUTPUT 6
GND	32		
		13	OUTPUT 7
GND	31		
		12	OUTPUT 8
GND	30		
		11	OUTPUT 9
GND	29		
		10	OUTPUT 10
GND	28		
		9	OUTPUT 11
GND	27		
		8	OUTPUT 12
GND	26		
		7	OUTPUT 13
GND	25		
		6	OUTPUT 14
GND	24		
		5	OUTPUT 15
GND	23		
		4	OUTPUT 16
GND	22		
		3	N/C
GND	21		
		2	N/C
GND	20		
		1	EXTEN

III. PROGRAMMING INFORMATION

The 9740/DO card responds to word and longword transfers to the Control and Status register, 32-bit counter and FIFO. Word reads of the board identifier PROM are also supported. The card's memory map is shown below.

TABLE 3

PAS 9740/DO MEMORY MAP

BASE + 00	Reserved	Reserved	BASE + 01
02	Control/Status	Control/Status	03
04	Reserved	Reserved	05
06	Reserved	Reserved	07
08	Counter MS	Counter MS	09
0A	Counter LS	Counter LS	0B
0C	FIFO MS	FIFO MS	0D
0E	FIFO LS	FIFO LS	0F
10	Reserved	Reserved	11
12	Control/Status	Control/Status	13
14	Reserved	Reserved	15
16	Reserved	Reserved	17
18	Counter MS	Counter MS	19
1A	Counter LS	Counter LS	1B
1C	FIFO MS	FIFO MS	1D
1E	FIFO LS	FIFO LS	1F
20	ID PROM	V (56)	21
22		M (4D)	23
24		E (45)	25
26		I (49)	27
28		D (44)	29
2A		P (50)	2B
2C		A (41)	2D
2E		S (53)	2F
30		9 (39)	31
32		7 (37)	33
34		4 (34)	35
36		0 (30)	37
38		D (44)	39
3A		O (4F)	3B
3C		B (42)	3D
3E	IDPROM	0 (30)	3F
40	SECOND	COPY	7F
80	THIRD	COPY	AF
B0	FORTH	COPY	FF

Control and Status Register

The Control and Status register is located at the cards base address plus 2. Writes to the Control register are used to set the states of the LEDs and SYSFAIL line, and to enable the output drivers and the counter.

Bit 0 of the control register steers the FAIL LED and SYSFAIL line on the backplane, if J28 is installed. When the card is reset the FAIL LED will come on, and the SYSFAIL line will be driven true. Writing a one to bit 0 can turn off the LED and the SYSFAIL line. Clearing bit 0 will also reset the FIFO, the time compare register, the 32-bit counter, and the output data register. In order for the card to operate normally, bit 0 must be set to a one.

Bit 1 of the control register will control the PASS LED if this function is selected with J27. This LED will be turned off when the board is reset or when a zero is written to bit 1. Writing a one to bit 1 can turn on the LED.

Bit 3 of the control register is used to enable the RS-232 output drivers when it is set to a one, and to disable the drivers when it is set to a zero. The card powers up with the output drivers disabled. TTL outputs are always enabled, and this bit does not affect the outputs.

Bit 4 of the control register is used to enable the counters, when it is set to a one, and disable the counters when it is set to zero.

Reading the card's base address plus two accesses the status register. Bits 0,1,3 and 4 of the status register read back the corresponding bits of the control register.

Bit 2 of the status register is the sequencer enable bit and indicates the card is enabled to generate output data patterns, when it is set. In order for the sequencer enable bit to set, the counter enable bit (bit 4) in the control register must be set, and the external clock enable signal must be true. Refer to description of J30 and J31 for more information on the external clock enable signal.

Bits 5, 6 and 7 indicate the status of the FIFO, and these bits are low true, (reading a zero indicates a true condition). Bit 5 is FIFO Empty, Bit 6 is FIFO Half Full and Bit 7 is FIFO Full.

TABLE 4

Status Register

7	6	5	4	3	2	1	0
FF Full LT	FF H Full LT	FF Empty LT	Cntr Enable HT	Out Enable HT	Seq Enable HT	Pass LED HT	Fail LED LT

LT = Low True
HT = High True

The power up or reset condition of the status register is FFC0, and indicates the FIFO is empty, the outputs are disabled, the sequencer is disabled, the PASS LED is off, (if selected with J27), and the FAIL LED is on.

32 Bit Counter

The 32 bit counter can be written to and read at the card's base address plus 8. A 1 MHz clock is used to increment this counter, which provides a count length of approximately 4294 seconds, before the counter rolls over. This register can only be accessed when the card is not generating output data patterns. In order for the card to generate output data patterns, the counter enable bit must be set in the control register, and the external clock enable signal must be true.

The counters can be used as a 32 bit test register when the card is not enabled to generate output data patterns. This feature is useful for checking out the card's VME bus interface.

FIFO

The FIFO can be written to at the card's base address plus C. The FIFO requires two 32 bit locations of information be written to define each output transition. The first location contains the time value when the data pattern will be driven, and the second location contains the data value that will be driven.
The time value is 32 bits wide and can be written either with a single 32-bit transfer, or with 2, 16-bit transfers. In either case the FIFO counter is incremented when the least significant sixteen bits are written. The output data is only sixteen bits wide, and is written to the most significant sixteen bits in the FIFO. The data value can be written with either a 32-bit transfer, or 2, 16 bit transfers, but the entire 32-bit width of the FIFO must be written to keep the FIFO properly aligned.

The FIFO can be written either when the sequencer is enabled or disabled. The status of the FIFO must be known prior to writing any data to it. ***If the FIFO is full, and the VME bus writes to it, that data will be lost.*** The FIFO will begin accepting data again when a new storage location becomes available. The FIFO is read by the on board sequencer, when the sequencer is enabled.
The sequencer will only read the FIFO when it contains valid time and output data.

Board Identifier PROM

The board identifier PROM is located at an offset of 20 (hex) from the base address, and can be read with word reads only. Only the least significant byte of the word will contain valid data, and the most significant byte will contain FF. The ID PROM contains 16 ASCII characters that specify the board's model number and revision level. A write to the ID PROM location will handshake, but not transfer any data.

A second, third and fourth copy of the board's registers are contained at offsets 40 through FF.

Generating Output Patterns

In order to generate an output data pattern the FIFO needs to be loaded with the time and output data values that define the data pattern. The time needs to be set by writing the counter, and writing to the control register enables the output drivers and sequencer. Once the sequencer is enabled, the first time value will be monitored until it matches the counter value. When a time match occurs, the data value will be presented to the output drivers, and the sequencer will monitor the new time value for the next time match. As the sequencer unloads the FIFO, the VME bus can write more data into the FIFO, after reading the status register to make sure the FIFO is not full.

Multiple Board Systems

In systems that require more than one pattern generator board, one board should be configured to drive the external enable line, and all the other boards should be configured to monitor this line. Refer to the description of J30 and J31 for more information. The clock select jumper, (J29), should be set to position 2-3 in multiple board systems, so that all boards are clocked from the 16 MHz backplane clock.