
**PAS 9742/DO
ENGINEERING SPECIFICATION**

**RECEIVER GATE GENERATOR
VME DIGITAL OUTPUT CARD
Revision A (08/08/2002)**

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Receiver Gate Generator VME Digital Output Card

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Receiver Gate Generator VME Digital Output Card

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I. INTRODUCTION

GENERAL DESCRIPTION

The PAS 9742/DO is a VME based, pulse generator and eight-channel analog output card. This card generates two digital output signals in response to a sync pulse input. These two TTL level output signals are known as Receiver Gate, (RG) and Time of Arrival, (TOA). Two, 32 bit wide registers on the card, which are written to over the VME bus, control the width of the pulses. The card also provides eight, twelve bit analog output channels.

VME systems with A16, A24, or A32 addressing, and data bus widths of 16 and 32 bits are supported. The pulse control and analog output registers only support thirty-two bit transfers. The other registers on the card use byte or word transfers. DIPswitches are used to configure the width of the address bus, and the instruction determines the width of the data transfer. A board identifier PROM, and a Control and Status register registers are also provided.

Card Features: PAS 9742/DO

- Receiver Gate (RG) and Time Of Arrival (TOA) output signals triggered by Sync input
- Width of RG and TOA is controlled by 32 bit registers written from the VME bus
- Pulse Width resolution is 1 microsecond
- TOA signal is a re-triggerable one shot, RG signal is non re-triggerable
- A multiplexer selects the Receiver Gate or the Pulse signal to drive the MSMT connector
- Eight each, twelve bit voltage output DAC's controlled by the VME bus
- DAC outputs are 0 to 10 Volts with 10 mA output drive current capability
- Input / Output lines are terminated on 16 SMC connectors at the front panel
- Board identifier PROM; ID code is VMEID PAS9742DO *. (* Is revision level)
- Four LEDs at the front panel provide the following status:
Pass, Fail, Pulse Enable, Multiplexer Select
- VME SYSFAIL asserts on power up, jumper selectable
- VME access: D32, D16, A32, A24, A16 Slave
- VME interrupts, none
- VME 6U form factor; 233 mm x 160 mm card size.

II. SPECIFICATIONS

Electrical Specifications

Number of Pulse Out Channels	2
Number of Test Points	3
Number of Input Signals	3
Number of Analog Outputs	8

Output Characteristics

Pulse Outputs and Test Points

Low Level Output Current	64 mA
High Level Output Current	-15 mA
Low Level Output Voltage @ IOL = 48 mAmps	0.35 V (typ.), 0.5 V (max.)
High Level Output Voltage @ IOH = -3 mA	2.4 V (min.), 3.2 V (typ.)
High Level Output Voltage @ IOH = -15 mA	2.0 V (min.)
Output Polarity	High True

Analog Output Channels

Output Range	0 to 10 Volts
Resolution	12 bits
Output Current	10 mA (into 1 K ohm load)
Integral Linearity Error	+/- 1 LSB (max)
Differential Linearity Error	+/- 1 LSB (typ)
Settling Time	10 uSec (typ)
Throughput Rate	
One Channel	100 KHz
All Channels, Combined	100 KHz
Output at Reset	0 Volts
Gain Drift	20 ppm / Degrees Celsius (typ)
Card Power Requirements	5 Volts @ 1 Amp (typ)
VMEbus Compliance	Fully compatible with VMEbus standard
Address Range	A32, A24, and A16 switch selectable
Address Block Size	256 consecutive byte locations
Data Width	D32, D16,
Interrupts	none

Environmental Specifications

Operating Temperature Range	-20 to 71 degrees Celsius with forced air cooling.
Storage Temperature Range	-40 to 85 degrees C.
Relative Humidity Range	0% to 100%, non-condensing

Physical Specifications

Dimensions	Form factor: 6U (160 mm x 233 mm)
Weight	12 oz. (typ)
Connectors	2 ea. 96 pos. DIN (VME bus connectors) 16 ea. SMC subminiature coaxial connectors, (AEP # 1110-1511-000 or equivalent)

Jumpers and Switches

The 9742/DO card contains two eight position DIPswitches, one ten position DIPswitch and one jumper wire. The three DIPswitches are used to set the board's VME base address, and are defined in Table 2 on page 9. When a switch is closed, the corresponding address bit must be low to select the card's address, and when a switch is open, the corresponding address bit must be high. The card is shipped configured for address F0000000.

Jumper wire JW4 allows the SYSFAIL line to be driven with bit 0 of the control register. The board is shipped with this jumper installed.

Switches S2-9 and S2-10 are used to select the boards operating environment, A16, A24 or A32, and the setting of these switches is defined in table 1.

TABLE 1
Address Modifiers

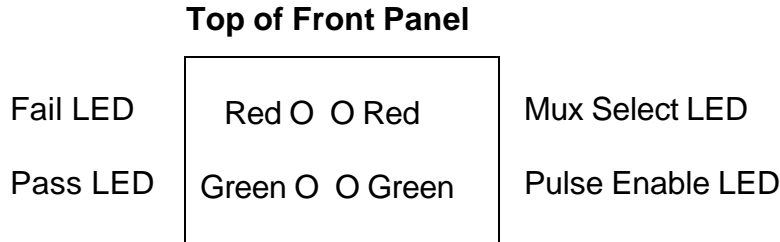
S2-10	S2-9	Address Modifiers	Address Space
Closed	Closed	09, 0D	Extended I/O
Closed	Open	29, 2D	Short I/O
Open	Closed	39, 3D	Standard I/O
Open	Open	29, 2D	Short I/O

TABLE 2
Jumper Plug and Switch Definitions

<u>Jumper #</u>	<u>Function</u>
JW4 IN	SYSFAIL controlled by control register
SW1-1	A8
SW1-2	A9
SW1-3	A10
SW1-4	A11
SW1-5	A12
SW1-6	A13
SW1-7	A14
SW1-8	A15
SW2-1	A16
SW2-2	A17
SW2-3	A18
SW2-4	A19
SW2-5	A20
SW2-6	A21
SW2-7	A22
SW2-8	A23
SW3-1	A24
SW3-2	A25
SW3-3	A26
SW3-4	A27
SW3-5	A28
SW3-6	A29
SW3-7	A30
SW3-8	A31

LED Indicators

Four LED's arranged in a 2 by 2 array are provided at the front panel to indicate the board's status. The position of the LED's is shown bellow.



The red Fail LED powers up on and is controlled with bit 0 of the control register. Writing a one to bit 1 will turn it off. The SYSFAIL line will also be driven when the FAIL LED is on, if J1 is installed.

The green Pass LED powers up off and is controlled by bit 1 of the control register. Writing a one to bit 1 will turn it on. This LED can be used to indicate the board has passed some initial power up tests.

The red Multiplexer Select LED powers up off and is controlled with bit 2 in the control register. Writing a one to bit 2 will turn it on. When the LED is off, the receiver gate signal drives the MSMT connector. When the LED is on, the pulse signal drives the MSMT connector.

The green Pulse Enable LED powers up off and is controlled with bit 3 of the control register. Writing a one to bit 3 will turn it on. When the LED is off, the board is disabled from generating pulses. When the LED is on the board is enabled to drive the RG and TOA pulse signals.

Connector Definitions

Two 96 position DIN connectors are installed on the backplane end of the board to make the standard VME bus connection. P1 is the upper connector and connects to the first 16 data lines, 24 address lines and the control signals. P2 is the lower connector and connects to an additional 16 data lines and 8 address lines to complete the A32, D32 VMEbus interface.

Sixteen SMA subminiature coaxial connectors are installed through the board's front panel to provide access to the I/O channels. Connector J3 is the top connector, and connector J18 is the bottom connector. The function of these connectors is defined on the following page.

TABLE 3
SMC Connector Definitions

J3	TOA
J4	TOATP
J5	MSMT
J6	MSMTTP
J7	SYNCTP
J8	SYNCI
J9	PULSE
J10	10 MHz
J11	AO 0
J12	AO 1
J13	AO 2
J14	AO 3
J15	AO 4
J16	AO 5
J17	AO 6
J18	AO 7

III. PROGRAMMING INFORMATION

The 9742/DO card responds to byte, word and longword transfers to the data port registers. Word and byte transfers to the control registers and the board identifier PROM are also supported. The card's memory map is shown below, and occupies 256 bytes of VME memory.

TABLE 4
PAS 9742/DO MEMORY MAP

BASE A+000	RESERVED	V (56)	001
002	RESERVED	M (4D)	003
004	RESERVED	E (45)	005
006	RESERVED	I (49)	007
008	RESERVED	D (44)	009
00A	RESERVED	P (50)	00B
00C	RESERVED	A (41)	00D
00E	RESERVED	S (53)	00F
000	RESERVED	9 (39)	011
012	RESERVED	7 (37)	013
014	RESERVED	4 (34)	015
016	RESERVED	2 (32)	017
018	RESERVED	D (44)	019
01A	RESERVED	O (4F)	01B
01C	RESERVED	A (41)	01D
01E	RESERVED	0 (30)	01F
020	RESERVED	RESERVED	021
07E	RESERVED	RESERVED	07F
080	RESERVED	CONTROL & STATUS	081
082	RESERVED	RESERVED	083
084	RECEIVER GATE MS	RECEIVER GATE MS	085
086	RECEIVER GATE LS	RECEIVER GATE LS	087
088	TIME OF ARRIVAL MS	TIME OF ARRIVAL MS	089
08A	TIME OF ARRIVAL LS	TIME OF ARRIVAL LS	08B
08C	RESERVED	RESERVED	08D
08E	RESERVED	RESERVED	08F
090	ANALOG OUTPUT 0	ANALOG OUTPUT 0	091
092	ANALOG OUTPUT 1	ANALOG OUTPUT 1	093
094	ANALOG OUTPUT 2	ANALOG OUTPUT 2	095
096	ANALOG OUTPUT 3	ANALOG OUTPUT 3	097
098	ANALOG OUTPUT 4	ANALOG OUTPUT 4	099
09A	ANALOG OUTPUT 5	ANALOG OUTPUT 5	09B
09C	ANALOG OUTPUT 6	ANALOG OUTPUT 6	09D
09E	ANALOG OUTPUT 7	ANALOG OUTPUT 7	09F
0A0	RESERVED	RESERVED	0A1
0FE	RESERVED	RESERVED	0FF

Board Identifier PROM (Base Address + 001H to 01FH) Read Only

The Board Identifier PROM is located starting at the board's base address plus 1, and continues to the base address plus 1F.

Byte and word reads to the Identifier PROM are supported. Only the least significant byte of a word read will contain valid data, and the most significant byte will contain FF. The ID PROM contains 16 ASCII characters that specify the board's model number and revision level. A write to the ID PROM location will handshake, but not transfer any data.

Control & Status Register (Base Address + 081H) Read / Write

The Control & Status Register, (CSR), provides four bits that are used to set the states of the front panel LED's. These bits also control the state of the SYSFAIL, multiplexer select and pulse enable lines. Four additional bits provide the functions of: software reset, clock select, loop back, and simultaneous DAC update. The format of this register is shown below.

TABLE 5

Control & Status Register

7	6	5	4	3	2	1	0
Update DAC's	Loop Back	Clock Select	Soft Reset	Pulse Enable	Mux Select	Pass LED	Fail LED

Bit 0 of the CSR steers the Fail LED at the front panel. The SYSFAIL line on the backplane will also be asserted if J1 is installed, and bit 0 is reset. When the card is reset the Fail LED will come on. Writing a one to bit 0 will turn off the LED and the SYSFAIL line. Reading bit 0 returns the state that was last written.

Bit 1 of the CSR controls the Pass LED. This LED will be turned off when the board is reset or when a zero is written to bit 1. Writing a one to bit 1 will turn on the LED. Reading bit 1 returns the state that was last written.

Bit 2 of the CSR controls the multiplexer select line, and determines if the Receiver Gate or Pulse input signal will appear on the MSMT output connector. When the board is reset or a zero is written to bit 2 the receiver gate signal will be selected to drive the MSMT output connector. Writing a one to bit 2 will select the pulse signal to drive the MSMT output connector. When bit 2 is a set to a one, the red Multiplexer Select LED will also turn on. Reading this bit returns the value that was last written to it.

Bit 3 of the CSR enables the board to generate the receiver gate and TOA pulses. When the board is reset or a zero is written to bit 3 the board is disabled from generating pulses. Writing a one to bit 3 will enable pulse generation. When bit 3 is set to a one, the green Pulse Enable LED will also turn on. Reading this bit returns the value that was last written to it.

Bit 4 of the CSR controls the software-reset function. Writing a one to bit 4 will reset the board with a pulse. Reading bit 4 will always return a zero. When a software reset is performed, the registers on the card will reset to the following states;

The CSR will be cleared to 00H

The Receiver Gate Register will be cleared to 00000000H,

The Time Of Arrival Register will be cleared to 00000000H.

All DAC's will be cleared to 0000H, 0.000 Volts

Bit 5 of the CSR controls the clock select line, and determines if the 10 MHz or 16 MHz backplane clock will be used to generate the internal 1 MHz clock. When the board is reset, or a zero is written to bit 5 the 10 MHz clock is used. Writing a one to bit 5 will select the 16 MHz clock. Selecting the 16 MHz clock is useful for testing the board in systems where the 10 MHz clock is not available. Reading this bit returns the value that was last written to it.

Bit 6 of the CSR will return the value that was last written. This bit has no other function.

Bit 7 of the CSR is used to update the D-to-A Converters. The DAC's have an input register and a DAC register. When bit 7 is cleared to a zero, the DAC register will track the input register, and the DAC output voltage will change whenever a new value is written to the DAC. When bit 7 is set to a one, new values written to the DAC will not change the DAC output voltage.

This bit is useful for updating all of the DAC voltages simultaneously. All of the input registers can be written with new values, while bit 7 of the CSR is set to one. Writing a zero to bit 7 of the CSR will cause all of the DAC output voltages to change at the same time.

The reset condition of this bit is zero, and it will return the value that was last written to it.

Receiver Gate Register (Base Address + 084H) Read / Write

The Receiver Gate, (RG), register is a 32 bit register and is used to control the width of the Receiver Gate output pulse. Writing a value to this register defines the pulse width in microseconds. When the Sync pulse is received, a low true pulse will be generated on the Receiver Gate output as defined by the value in this register. If another Sync pulse is received before the RG pulse has expired, the pulse width will not be extended. This mode of operation allows the RG logic to act as a digitally controllable non re-triggerable one shot.

The Receiver Gate register supports word and long word transfers. Reading this register will return the value last written to it.

Time Of Arrival Register (Base Address + 088H) Read / Write

The Time Of Arrival, (TOA), register is a 32 bit register and is used to control the width of the Time Of Arrival output pulse. Writing a value to this register defines the pulse width in microseconds. When the Sync pulse is received, a low true pulse will be generated on the Time Of Arrival output as defined by the value in this register. If another Sync pulse is received before the TOA pulse has expired, the pulse width will be extended by the amount of time defined in the TOA register. This mode of operation allows the TOA logic to act as a digitally controllable re-triggerable one shot.

The Time Of Arrival register supports word and long word transfers. Reading this register will return the value last written to it.

Eight D to A Converters (Base Address + 90H thru 9EH) Read / Write

The eight Digital to Analog Converters, (DAC's) can be written to starting at the board's base address plus 90 (hex). Offset binary data should be used when writing the DAC's, since the sign of the data is always positive. A digital output word of 0FFF produces positive full scale. Zero volts is produced with a digital word of 0000, and half scale occurs at 0800 (hex).

The D to A converters can be written to individually using word transfers, or in pairs using long word transfers. Reading the D-to-A Converters will return the twelve least significant bits that were last written. The four most significant bits will all return ones, or an F (hex).