
**PAS 9760/DI
ENGINEERING SPECIFICATION**

**16 BIT CHANGE OF STATE
WITH 1 μ SEC TIME STAMPING
VME DIGITAL INPUT CARD
Revision D (04/24/2002)**

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Precision Analog Systems Co.
7540 NW 5th Street - Suite 2
Plantation, Florida 33317
Phone: (954) 587-0668
Fax: (954) 587-0665
E-mail: LNA@precisionanalog.com

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16 Bit Change of State with 1 uSec Time Stamping VME Digital Input Card

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16 Bit Change of State with 1 uSec Time Stamping VME Analog Output Card

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I. INTRODUCTION

GENERAL DESCRIPTION

The PAS 9760/DI is a VME based, 16 channel, digital input card with Change of State (COS) detection and 1 uSec time stamping. Each time a change of state is detected, the card will store the state of the input signals and a time value in an on board FIFO. A VME interrupt will also be generated for the first COS if interrupts are enabled. This card can be used in VME systems with A16, A24, or A32 addressing, and data bus widths of 16 and 32 bits are supported. Pluggable jumpers are used to configure the width of the address and data buses. The input signals are connected to a 37 pin D connector mounted through the front panel. A board identifier PROM, interrupt vector register, and control register are provided in addition to the 31 bit 1, uSec counter and 512 by 32 FIFO.

Card Features: PAS 9760/DI

- TTL compatible input channels, with schmitt triggers
- Input signals on DB37 female connector at the front panel
- Detects change of state on low to high transition or high to low transition
- Time stamps every transition with 1 uSec resolution, and stores data and time stamp in a FIFO. This FIFO is 32 bits wide by 512 words deep
- A VME interrupt will be generated on the first COS, if interrupts are enabled
- VME bus can read 16 bits of data and 16 LS bits of time with 1, 32-bit read. Wider time read of 32 bits is stored in the FIFO behind the time and data word
- Time can be set with a VME write, counters are enabled with a control word write
- One board can be designated the master and used to enable all other counters in the system. All of the counters can be clocked from the VME system clock or from their on board oscillators
- Status register contains the following bits; Pass, Fail, Interrupt Enable, Interrupt Pending, Counter Enabled, FIFO Empty, FIFO Half Full, FIFO Full
- VME 6U form factor; 233 mm x 160 mm card size
- VME access: D32, D16; A32, A24, A16 Slave. VME Interrupter
- Optional VME SYSFAIL assert on power up, SYSFAIL LED and Board Access LED on front panel
- Board identifier PROM; ID code is VMEID PAS9760DI ** (** is revision level)

II. SPECIFICATIONS

Electrical Specifications

Number of Channels	16
Nominal Input Voltage Range	0 to 12 Volts
High Level Input Voltage	2.0 Volts (min.)
Low Level Input Voltage	0.8 Volts (max.)
Input Over-Voltage Protection	+ 75 Volts
Card Power Requirements	5 Volts @ 2 Amps (typ)

Environmental Specifications

Operating Temperature Range	0 to 60 degrees Celsius with forced air-cooling.
Storage Temperature Range	-20 to 85 degrees C
Relative Humidity Range	20% to 80%, non-condensing

Physical Specifications

Dimensions	Form factor: Double (160 mm x 233 mm)
Weight	16 oz. (typ)
Connectors	2 ea. 96 pos. DIN (VME bus connectors) 1 ea. DB37 female (input data connector)

Jumpers and Indicators

The 9760/DI card contains 36 Pluggable jumpers and two LED indicators. The first 24 jumpers are used to set the board's VME base address, and are defined in the table on page 5. When a jumper is installed, the corresponding address bit must be low to select the card's address, and when a jumper is removed the corresponding address bit must be high. The card is shipped configured for address F0000000, so that 20 of the possible 24 address jumpers are installed. J1-J20 are installed, J21-J24 are removed.

Jumpers J25 and J26 are used to select the boards operating environment, either A16, A24 or A32, and the installation of these jumpers is defined in table 1. J25 and J26 are installed for shipment, to select 32-bit addressing.

Jumper J27 is used to set the function of the Pass/Access LED. When it is installed in position 1-2, the LED is controlled by bit 1 in the control register. When J27 is in position 2-3 the LED indicates the board is being accessed. The card is shipped with J27 in position 2-3.

Jumper J28 allows the SYSFAIL line to be driven with bit 0 of the control register when it is installed. The card is shipped with J28 removed.

Jumpers J29, J30, and J31 are used to select the interrupt request level as defined below.

TABLE 1
Interrupt Request Level

J31	J30	J29	Interrupt Level
IN	IN	IN	Invalid
IN	IN	OUT	1
IN	OUT	IN	2
IN	OUT	OUT	3
OUT	IN	IN	4
OUT	IN	OUT	5
OUT	OUT	IN	6
OUT	OUT	OUT	7

The card is shipped with interrupt level 4 selected.

Jumpers 32 and 33 are reserved. They will be used to select which edge will generate a change of state. The card currently detects changes on both edges. The card is shipped with J32 and J33 in position 1-2.

Jumper J34 is used to select the source of the 16 MHz clock. When J34 is in position 1-2 the clock is supplied from the VME SYCLK line. When J34 is in position 2-3 the clock is supplied from an on board oscillator. The board is shipped with J34 in position 1-2.

Jumpers J35 and J36 are used to configure the external clock enable line.

When J35 is not installed, this card monitors the external clock enable input line. The line must be driven low by another card in the system, in order for the counters on this card to be enabled. When J35 is installed, the external clock enable line is always enabled. The card is shipped with J35 installed.

When jumper J36 is installed, this card will drive the external clock enable line, and all other cards in the system should be set to monitor this line. Only one card in a system should be set to drive the external clock enable line. The card is shipped with J36 removed.

TABLE 2
PLUGGABLE JUMPER DEFINITIONS

<u>Jumper #</u>	<u>Function</u>
J1	A8
J2	A9
J3	A10
J4	A11
J5	A12
J6	A13
J7	A14
J8	A15
J9	A16
J10	A17
J11	A18
J12	A19
J13	A20
J14	A21
J15	A22
J16	A23
J17	A24
J18	A25
J19	A26
J20	A27
J21	A28
J22	A29
J23	A30
J24	A31
J25 IN, J26 IN	A32 Addressing
J25 IN, J26 OUT	A24 Addressing
J25 OUT, J26 X	A16 Addressing
J27 (1-2)	LED 2 indicates board passed
J27 (2-3)	LED 2 indicates board accessed
J28 IN	SYSFAIL controlled by control register
J29, 30, 31	Interrupt Vector Level
J32, 33	Transition select
J34	16 MHz Clock Source
J35, 36	External clock enable

Two LEDs are provided at the front panel to indicate the board's status. The upper LED, (LED 1) is the Fail LED, and powers up on. This LED is controlled with bit 0 of the control register, and can be turned off by writing a one to bit 0. The SYSFAIL line will also be driven when LED 1 is on, if J28 is installed.

The lower LED, (LED 2), is the Pass/Access LED, and its function is selected with J27. When it is configured for the pass function, it is controlled by bit 1 of the control register. LED 2 can be turned on by writing a one to bit 1, and it will power up turned off. When configured for the access function, LED 2 will turn on any time the board is accessed. A one-shot is used to drive this LED, so that it will be visible on single cycle accesses.

Connector Definitions

Two 96 position DIN connectors are installed on the backplane end of the board to make the standard VME bus connection. A DB37 female connector is installed through the board's front panel to provide access to the sixteen input channels. The pin out of this connector is defined on the following page.

TABLE 3
DB37 Connector

GND	37	19	INPUT 1
GND	36	18	INPUT 2
GND	35	17	INPUT 3
GND	34	16	INPUT 4
GND	33	15	INPUT 5
GND	32	14	INPUT 6
GND	31	13	INPUT 7
GND	30	12	INPUT 8
GND	29	11	INPUT 9
GND	28	10	INPUT 10
GND	27	9	INPUT 11
GND	26	8	INPUT 12
GND	25	7	INPUT 13
GND	24	6	INPUT 14
GND	23	5	INPUT 15
GND	22	4	INPUT 16
GND	21	3	N/C
GND	20	2	N/C
		1	EXTEN

A Screw Termination Panel (STP) is available for terminating field signals and cabling them to the 9760/DI card. The model # for the STP is 9400, and the I/O cable is # CBLF-D37A-0010.

III. PROGRAMMING INFORMATION

The 9760/DI card responds to word and longword transfers to the Control and Status register, Interrupt Vector register, 31-bit counter and FIFO. Word reads of the board identifier PROM are also supported. The card's memory map is shown on the following page.

TABLE 4
PAS 9760/DI MEMORY MAP

BASE + 00	Reserved	Reserved	BASE + 01
02	Control/Status	Control/Status	03
04	Reserved	Reserved	05
06	Reserved	Int. Vector	07
08	Counter MS	Counter MS	09
0A	Counter LS	Counter LS	0B
0C	FIFO MS	FIFO MS	0D
0E	FIFO LS	FIFO LS	0F
10	Reserved	Reserved	11
12	Control/Status	Control/Status	13
14	Reserved	Reserved	15
16	Reserved	Int. Vector	17
18	Counter MS	Counter MS	19
1A	Counter LS	Counter LS	1B
1C	FIFO MS	FIFO MS	1D
1E	FIFO LS	FIFO LS	1F
20	ID PROM	V (56)	21
22	(FF)	M (4D)	23
24	(FF)	E (45)	25
26	(FF)	I (49)	27
28	(FF)	D (44)	29
2A	(FF)	P (50)	2B
2C	(FF)	A (41)	2D
2E	(FF)	S (53)	2F
30	(FF)	9 (39)	31
32	(FF)	7 (37)	33
34	(FF)	6 (36)	35
36	(FF)	0 (30)	37
38	(FF)	D (44)	39
3A	(FF)	I (49)	3B
3C	(FF)	C (43)	3D
3E	IDPROM	0 (30)	3F
40	SECOND	COPY	7F
80	THIRD	COPY	AF
B0	FORTH	COPY	FF

Control and Status register

The Control and Status register is located at the cards base address plus 2. Writes to the Control register are used to set the states of the LED's and SYSFAIL line, and to enable the counter and VME interrupts.

Bit 0 of the Control register steers the fail LED and acts as a board reset signal. The SYSFAIL line on the backplane will also be driven if J28 is installed. When the card is reset the fail LED will come on, and the SYSFAIL line will be driven true. Writing a one to bit 0 can turn off the LED and the SYSFAIL line. Clearing bit 0 will also reset the FIFO, and the 32-bit counter. **In order for the card to operate normally, bit 0 must be set to a zero.**

Bit 1 of the Control register will control the pass LED if this function is selected with J27. This LED will be turned off when the board is reset or when a zero is written to bit 1. Writing a one to bit 1 can turn on the LED.

Bit 3 of the Control register is used to enable VME interrupts when it is set to a one, and to disable interrupts when it is set to a zero.

Bit 4 of the Control register is used to enable the counters, when it is set to a one, and the external clock enable signal is true. (See information on J35 and J36).

Reading the card's base address plus 2 accesses the Status register. Bits 0,1 and 3 of the Status register read back the corresponding bits of the Control register.

Bit 2 of the Status register indicates a VME interrupt is pending, when it is set. The interrupt pending bit is cleared when the interrupt vector register is read.

Bit 4 of the Status register indicates the counters and sequencer have been enabled to monitor changes. This bit indicates bit 4 of the control register is set **and** the external clock enable signal is true.

Bits 5, 6 and 7 indicate the status of the FIFO, and these bits are low true, (reading a zero indicates a true condition). Bit 5 is FIFO Empty, Bit 6 is FIFO Half Full and Bit 7 is FIFO Full.

TABLE 5
Control and Status Register

7	6	5	4	3	2	1	0
FF Full LT	FF H Full LT	FF Emty LT	Cnt Enbl HT	Int Enbl HT	Int Pend HT	Pass LED HT	Fail LED LT Reset

LT = Low True
HT = High True

FIFO

The power up reset condition of the status register is FFC0, and indicates the FIFO is empty, the counter is disabled, the interrupts are disabled, the Pass LED is off, (if selected with J27), and the Fail LED is on. When the Fail LED is on the FIFO and the counters are cleared.

The interrupt vector register can be written to and read at the card's base address plus 4 with either word or longword transfers. This register is only a byte wide, so the most significant byte will return FF. This register is not affected by the reset bit (bit 0) in the control register.

The 31 bit counter can be written to and read at the cards base address plus 8, when the reset bit in the control register is false (bit 0 is a 1). A 1 MHz clock is used to increment this counter, which provides a count length of approximately 2147 seconds, before the counter rolls over. This register can only be accessed when the card is not armed to monitor change of state inputs. In order to arm the card, the counter enable bit must be set in the control register, and the external clock enable signal must be true. The counters can be used as a 31 bit test register, (bits 0-30), when the card is not monitoring input changes. The most significant bit, (bit 31), will always return a 1 when the counters are used as test registers. The test register feature is useful for checking out the card's VME bus interface.

The FIFO can be read at the card's base address plus C. The FIFO contains two 32-bit locations of data for each change that is detected. The first location contains the input data word in the most significant 16 bits, and the 16 LSBs of time on the least significant bits. The next location in the FIFO contains the 31-bit time value and an overflow status bit in the most significant bit. If the FIFO is full and a change of state is detected, the error bit will be set to a 1, and loaded into the FIFO, the next time a location becomes available. The error bit will reset the next time the FIFO is not full, and a change occurs that causes the FIFO to be written.

Whenever the FIFO is read, both long words need to be read, in order to keep the FIFO on an even boundary. Prior to reading the FIFO, the status register should be read to determine how full the FIFO is. **If the status register indicates that the FIFO is full, then the system is not keeping up with the process that is being monitored, and some changes will be lost.** By monitoring the error bit in the FIFO, the user can determine when an overflow condition occurred. **If the error bit is ever set, then the acquisition system is not keeping up with the process, and some changes have been lost.**

The only time valid data can be read from the FIFO is when the card is monitoring changes. In order for the card to monitor changes, the reset bit in the control register must be false, the counter enable bit must be set in the control register and the external clock enable signal must be true. After the card has been enabled, the onboard sequencer will load time and data values into the FIFO when it detects the inputs have changed state. If the card's interrupts are enabled, an interrupt request will be generated when the sequencer loads the FIFO with the first time / data pair, and the FIFO status changes from empty to not empty. The interrupt pending bit will set in the status register whenever the card is generating an interrupt request. The interrupt request and the interrupt pending status bit will be reset whenever the interrupt vector register is read.

If the FIFO ever gets full the sequencer will not load any new data into the FIFO and subsequent changes will be lost. When the FIFO is full and the sequencer attempts to write another time / data pair, an over flow bit will set and be written into the FIFO's most significant bit once space is available. Once the VME bus reads the FIFO, and space is available for another time / data pair, the sequencer will resume loading the FIFO.

Board Identifier PROM

The board identifier PROM is located at an offset of 20 (hex) from the base address, and can be read with word reads only. Only the least significant byte of the word will contain valid data, and the most significant byte will contain FF. The ID PROM contains 16 ASCII characters that specify the board's model number and revision level. A write to the ID PROM location will handshake, but not transfer any data.

A second, third and fourth copy of the board's registers are contained at offsets 40 through 7F, 80 through AF, and B0 through FF.