
**PAS 9780/DIO
ENGINEERING SPECIFICATION**

**DUAL TWELVE BY TWELVE MATRIX
VME DIGITAL INPUT / OUTPUT CARD
Revision A (02/27/2001)**

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Dual Twelve by Twelve Matrix VME digital Input / Output Card

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Dual Twelve by Twelve Matrix VME digital Input / Output Card

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I. INTRODUCTION

GENERAL DESCRIPTION

The PAS 9780/DIO card contains two by twelve matrix arrays. Each matrix has twelve input channels and twelve output channels. Logic on the card allows any of the input channels to be mapped to any of the output channels. Each matrix uses twelve registers that are accessible by the VME bus to steer the input channels to an output channel. Each output channel is assigned to one of these steering registers. When a bit in a given output steering register is true and the corresponding input is true, then that output will go true.

The steering registers also contain test and override bits for each output. If the test bit is true, then the override bit determines the state of the output. The override bit can be used to force the output true or false. The VME bus can also read the states of the inputs to the matrix.

The inputs and outputs can be set up to detect 28 Volts or ground with one jumper plug per matrix. When a matrix is set to detect ground, then ground is defined as the true or logic one state. When a matrix is set to detect 28 Volts, then 28 Volts is defined as the true or logic one state.

In the case where the card is set to detect ground, the input signals are pulled up to 28 Volts with 10 K resistors. The input buffers on the card are capable of withstanding 28 Volt signals. If an input signal is pulled low, and the corresponding bit in the output steering register is set to a one, then that output signal will be driven low with an open drain FET output driver. The output sink current is approximately 50 mA.

In the case where the card is set to detect 28 volts, the input signals are pulled to ground with 10 K resistors. If an input signal is driven to 28 Volts and the corresponding bit in the output steering register is set to a one, then that output signal will be driven to 28 Volts with a FET output driver. The output source current is approximately 25 mA.

An on board 30 Volt power supply is available as an option. This DC-to-DC converter steps up the 5 Volt backplane voltage to 30 volts at 500 mA. If more than 500 mA is required by the outputs, then 28 Volts can be connected to the card's I/O connectors. Two 50 position shrouded headers are used to terminate the I/O signals. One connector is used for each matrix and terminates twelve inputs and grounds, twelve outputs and grounds and a 28-volt supply input and ground.

VME systems with A16, A24, or A32 addressing are supported, which allows the card's base address to be located anywhere in the VME address range. Data transfers of 16 and 32 bits are supported, and the states of two steering registers can be read with a single longword transfer.

Card Features: PAS 9780/DIO

- Two twelve by twelve matrix arrays.
- Output steering registers allow any one or more inputs to drive any output.
- Value of steering register can be read back with VME input transfer.
- Outputs can be driven true or false with override and test bits for each output.
- Matrix input status can be read over the VME bus.
- Each matrix can be configured for 28 Volt or ground operation with a jumper plug.
- Matrix I/O on 2 ea. 50 position connectors, allows the use of mass termination cable.
- VME 6U form factor; 233 mm x 160 mm card size.
- VME access: D32, D16; A32, A24, A16 Slave.
- Optional VME SYSFAIL asserts on power up, jumper selectable.
- Four LED's provided on the front panel; Pass, Fail, CSR2 and CSR3 LED's
- Board Identifier PROM. (Board ID is VMEIDPAS9780DIOA)
- Operating temperature range; 0 to 60 deg. C.
- Board identifier PROM, and control and status registers.
- Four LEDs are provided at the front panel to display the board's status.

II. SPECIFICATIONS

Electrical Specifications

Number of Matrices per Card	2
Number of Input Channels Per Matrix	12
Number of Output Channels Per Matrix	12

Characteristics when the matrix is configured to detect ground on the inputs and sink current to ground on the outputs.

Input Impedance	8.5 K Ohms (typ.)
Open Circuit Input Voltage	25 Volts (typ.)
Logic Polarity	Ground = Logic One
Logic 1 Input Voltage	5 Volts (max)
Logic 0 Input Voltage	20 Volts (min)

Output Type	Open Drain FET
Output Sink Voltage	25 mV (typ) Iout less than 50 mA
Output Switch Impedance	0.5 Ohm (typ.)
Active Output Device	VN3205N3

Characteristics when the matrix is configured to detect 28 Volts on the inputs and source current to 28 Volts on the outputs.

Input Impedance	8.5 K Ohms (typ.)
Open Circuit Input Voltage	0 Volts (typ.)
Logic Polarity	+ 28 Volts = Logic One
Logic 1 Input Voltage	20 Volts (min.)
Logic 0 Input Voltage	5 Volts (max.)

Output Source Voltage	Vext – 50mV (typ) Vext = 28 Volts, Iout less than 50 mA
Output Switch Impedance	0.9 Ohm (typ.)
Active Output Device	VP2206N3
Card Power Requirements 5 Volts @	TBD Amp, (typ.)

Environmental Specifications

Operating Temperature Range	0 to 60 degrees C.
Storage Temperature Range	-20 to 85 degrees C.
Relative Humidity Range	20% to 80%, non-condensing

Physical Specifications

Dimensions	Form factor: Double (160 mm x 233 mm)
Weight	12 oz. (typ.)
Connectors	2 ea. 96 position, (VME bus connectors) 2 ea. 50 position, (Matrix Input / Output connectors)

Jumpers and Indicators

The 9780/DIO card contains 19 jumper plugs, a ten-position DIPswitch and four LED indicators. Sixteen of the jumpers and 8 positions of the DIP switch are used to set the board's VME base address, and are defined in the Table 1 on page 10. When a jumper is installed, or a switch is closed, the corresponding address bit must be low to select the card's address. When a jumper is removed, or a switch is open the corresponding address bit must be high. The card is shipped configured for address F0000000, so that 12 of the possible 16 address jumpers are installed.

Switches SW1-9 and SW1-10 are used to select the board's operating environment, A16, A24 or A32, and their setting is defined in Table 1 on page 10.

Jumper J1 allows the SYSFAIL line to be driven with bit 0 of the control register when it is installed.

Jumpers J3 and J4 are 3 pin jumper strips, and are used to configure whether the matrices sense ground or 28 Volts. The configuration of these jumpers is defined in Table 1 on page 7.

TABLE 1
PLUGGABLE JUMPER DEFINITIONS

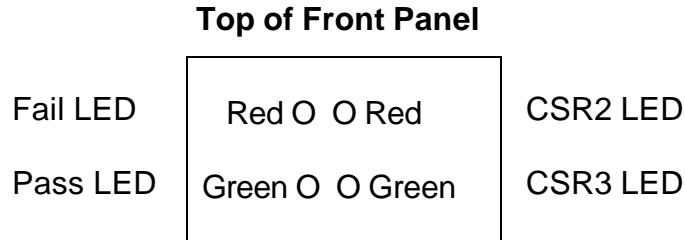
Jumper #	Function
J1 IN	SYSFAIL driven by bit 0 of CSR
J3, 1-2	Matrix A, Ground Sensing
J3, 2-3	Matrix A, 28 Volt Sensing
J4, 1-2	Matrix B, Ground Sensing
J4, 2-3	Matrix B, 28 Volt Sensing
SW1-1	A8
SW1-2	A9
SW1-3	A10
SW1-4	A11
SW1-5	A12
SW1-6	A13
SW1-7	A14
SW1-8	A15
SW1-9	Address space (See table below)
SW1-10	Address space (See table below)
J16	A16
J17	A17
J18	A18
J19	A19
J20	A20
J21	A21
J22	A22
J23	A23
J24	A24
J25	A25
J26	A26
J27	A27
J28	A28
J29	A29
J30	A30
J31	A31

TABLE 2
Address Modifiers

SW1-9	SW1-10	Address Modifiers	Address Space
Closed	Closed	09, 0D	Extended I/O
Closed	Open	39, 3D	Standard I/O
Open	Closed		Invalid
Open	Open	29, 2D	Short I/O

Front Panel LEDs

Four LED's arranged in a 2 by 2 array are provided at the front panel to indicate the board's status. The position of the LED's is shown below



The Fail LED powers up on, and is controlled with bit 0 of the control register. Writing a one to bit 0 can turn off this LED. The state of this LED is reflected in bit 0 of the status register. When the Fail LED is on, and J1 is installed, the SYSFAIL line will be driven on the VMEbus.

The Pass LED is controlled by bit 1 of the control register. This LED can be turned on by writing a one to bit 1, and it will power up turned off. Bit 1 in the status register reflects the state of this LED. Once the board has passed some initial power up tests this LED can turned on to indicate successful completion of the power up sequence.

The CSR 2 LED is controlled by bit 2 of the control register. This LED can be turned on by writing a one to bit 1, and it will power up turned off. Bit 2 in the status register reflects the state of this LED.

The CSR 3 LED is controlled by bit 3 of the control register. This LED can be turned on by writing a one to bit 3, and it will power up turned off. Bit 3 in the status register reflects the state of this LED.

Connector Definitions

Two 96 position DIN connectors are installed on the backplane end of the board to make the standard VME bus connection. A pair of 50 position, shrouded headers is installed through the board's front panel to provide access to the two twelve by twelve matrix arrays. The pin definitions of these connectors provided below and on the following page.

TABLE 3

Matrix A I/O Connector P3

Top Connector

Pin Numbers			
GND	50	49	IN 0A
GND	48	47	IN 1A
GND	46	45	IN 2A
GND	44	43	IN 3A
GND	42	41	IN 4A
GND	40	39	IN 5A
GND	38	37	IN 6A
GND	36	35	IN 7A
GND	34	33	IN 8A
GND	32	31	IN 9A
GND	30	29	IN 10A
GND	28	27	IN 11A
GND	26	25	OUT 0A
GND	24	23	OUT 1A
GND	22	21	OUT 2A
GND	20	19	OUT 3A
GND	18	17	OUT 4A
GND	16	15	OUT 5A
GND	14	13	OUT 6A
GND	12	11	OUT 7A
GND	10	9	OUT 8A
GND	8	7	OUT 9A
GND	6	5	OUT 10A
GND	4	3	OUT 11A
GND	2	1	EXT PWR

TABLE 4
Matrix B I/O Connector P4
Bottom Connector

Pin Numbers			
GND	50	49	IN 0B
GND	48	47	IN 1B
GND	46	45	IN 2B
GND	44	43	IN 3B
GND	42	41	IN 4B
GND	40	39	IN 5B
GND	38	37	IN 6B
GND	36	35	IN 7B
GND	34	33	IN 8B
GND	32	31	IN 9B
GND	30	29	IN 10B
GND	28	27	IN 11B
GND	26	25	OUT 0B
GND	24	23	OUT 1B
GND	22	21	OUT 2B
GND	20	19	OUT 3B
GND	18	17	OUT 4B
GND	16	15	OUT 5B
GND	14	13	OUT 6B
GND	12	11	OUT 7B
GND	10	9	OUT 8B
GND	8	7	OUT 9B
GND	6	5	OUT 10B
GND	4	3	OUT 11B
GND	2	1	EXT PWR

III. PROGRAMMING INFORMATION

The 9780/DIO card responds to word and longword transfers to the two matrices. Word writes to the control register and word reads of the status register and board identifier PROM is also supported. The card's memory map is shown on the following page.

TABLE 5
PAS 9780/DIO MEMORY MAP

BASE + 000	RESERVED	V (56)	001
002	RESERVED	M (4D)	003
004	RESERVED	E (45)	005
006	RESERVED	I (49)	007
008	RESERVED	D (44)	009
00A	RESERVED	P (50)	00B
00C	RESERVED	A (41)	00D
00E	RESERVED	S (53)	00F
000	RESERVED	9 (39)	011
012	RESERVED	7 (37)	013
014	RESERVED	8 (38)	015
016	RESERVED	0 (30)	017
018	RESERVED	D (44)	019
01A	RESERVED	I (49)	01B
01C	RESERVED	O (4F)	01D
01E	RESERVED	A (41)	01F
020	RESERVED	RESERVED	021
07E	RESERVED	RESERVED	07F
080	RESERVED	CONTROL & STATUS	081
082	RESERVED	RESERVED	083
09E	RESERVED	RESERVED	09F
0A0	STEERING REG OUTPUT 0 A		0A1
0A2	STEERING REG OUTPUT 1 A		0A3
0A4	STEERING REG OUTPUT 2 A		0A5
0A6	STEERING REG OUTPUT 3 A		0A7
0A8	STEERING REG OUTPUT 4 A		0A9
0AA	STEERING REG OUTPUT 5 A		0AB
0AC	STEERING REG OUTPUT 6 A		0AD
0AE	STEERING REG OUTPUT 7 A		0AF
0B0	STEERING REG OUTPUT 8 A		0B1
0B2	STEERING REG OUTPUT 9 A		0B3
0B4	STEERING REG OUTPUT 10 A		0B5
0B6	STEERING REG OUTPUT 11 A		0B7
0B8	MATRIX INPUTS A		0B9
0BA	RESERVED	RESERVED	0BB
0BE	RESERVED	RESERVED	0BF

TABLE 5 CONT.
PAS 9780/DIO MEMORY MAP

0C0	STEERING REG OUTPUT 0 B		0C1
0C2	STEERING REG OUTPUT 1 B		0C3
0C4	STEERING REG OUTPUT 2 B		0C5
0C6	STEERING REG OUTPUT 3 B		0C7
0C8	STEERING REG OUTPUT 4 B		0C9
0CA	STEERING REG OUTPUT 5 B		0CB
0CC	STEERING REG OUTPUT 6 B		0CD
0CE	STEERING REG OUTPUT 7 B		0CF
0D0	STEERING REG OUTPUT 8 B		0D1
0D2	STEERING REG OUTPUT 9 B		0D3
0D4	STEERING REG OUTPUT 10 B		0D5
0D6	STEERING REG OUTPUT 11 B		0D7
0D8	MATRIX INPUTS B		0D9
0DA	RESERVED	RESERVED	0DB
0FE	RESERVED	RESERVED	0FF

Board Identifier PROM (Base Address + 001H to 01FH) Read Only

The Board Identifier PROM is located starting at the board's base plus 1, and continues to the base address plus 1F. Byte and word reads to the Identifier PROM are supported.

Only the least significant byte of a word read will contain valid data, and the most significant byte will contain FF. The ID PROM contains 16 ASCII characters that specify the board's model number and revision level. A write to the ID PROM location will handshake, but not transfer any data.

TABLE 6
Control and Status Register (base + 81)

7	6	5	4	3	2	1	0
Loop Back	Loop Back	loop Back	SW Reset Pulse	CSR3 LED	CSR2 LED	Pass LED	Fail LED

Bit 7-5 Loopback. These bits will return the value last written to them.

Bit 4 Writing a 1 to this bit will generate a software-reset pulse. This bit will always return a 0 when read. Following a software reset, the CSR and all the functional bits in the output steering registers will return zeros.

Bit 3 This bit controls the CSR3 LED, and returns the value last written to it.

- 1 = Turn on the CSR3 LED
- 0 = Turn off the CSR3 LED

Bit 2 This bit controls the CSR2 LED, and returns the value last written to it.

- 1 = Turn on the CSR2 LED
- 0 = Turn off the CSR2 LED

Bit 1 This bit controls the Pass LED, and returns the value last written to it.

- 1 = Turn on the Pass LED
- 0 = Turn off the Pass LED

Bit 0 This bit controls the Fail LED, and returns the value last written to it. The SYSFAIL line will also be asserted when the Fail LED is on if J1 is installed.

- 1 = Turn off the Fail LED
- 0 = Turn on the Fail LED

**Output Steering Registers Matrix A (base + AO to B6)
Output Steering Registers Matrix B (base + CO to D6)**

These registers are used to define which inputs will be steered to a given output. There are two sets of registers; one set for matrix A and the other set for matrix B. Each set contains twelve registers, one for each output channel in the matrix. The addresses of these registers are provided in the table on page 10.

When a bit is set to a one in one of the output steering registers, AND the input associated with that bit is true, the output will be driven true. Matrices configured to detect ground define ground as the true or logic one state. Matrices configured to detect 28 Volts define 28 Volts as the true or logic one state. More than one input can be used to drive any output. As an example, if bits 4, 7 and 9 were set to ones in output steering register 3, AND any one of the inputs 4, 7 OR 9 are driven true, output 3 will be driven true.

The override bit for each register is bit 12, and the test bit is bit 13. When bit 13 is set to a one, the output is in test mode, and the state of the output is controlled by bit 12. The override bit can be used to force the output true or false.

The state of the output steering registers can be read back over the VME bus. Bits zero through thirteen will return the value last written. Bits fourteen and fifteen will always return ones.

TABLE 7
Output Steering Registers Matrix

15	14	13	12	11	10	9	8
Not Used	Not Used	Test	Over Ride	Input 11	Input 10	Input 9	Input 8

7	6	5	4	3	2	1	0
Input 7	Input 6	Input 5	Input 4	Input 3	Input 2	Input 1	Input 0

**Input Register Matrix A (base + B8)
Input Register Matrix B (base + D8)**

These registers are used to read the state of the input signals to each matrix.

TABLE 8
Input Register Matrix

15	14	13	12	11	10	9	8
Not Used	Not Used	Not Used	Polar Jmp	Input 11	Input 10	Input 9	Input 8

7	6	5	4	3	2	1	0
Input 7	Input 6	Input 5	Input 4	Input 3	Input 2	Input 1	Input 0

Bits 0 through 11 return the state of the inputs of the matrix and bit 12 returns the state of the polarity jumper. Bits 13 through 15 return ones when read.

When the matrix is configured to detect 28 Volts, the polarity bit will return a one. In this configuration all inputs that are at 28Volts will return ones in their respective input bits, and all inputs that are at ground will return zeros.

When the matrix is configured to detect ground, the polarity bit will return a zero. In this configuration all inputs that are at ground will return ones in their respective input bits, and all inputs that are at 28 Volts will return zeros.