
**PAS 9819/AO
ENGINEERING SPECIFICATION**

**VME 4 CHANNEL, 16 BIT ISOLATED
CURRENT OUTPUT CARD
Revision A**

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VME 4 Channel 16 Bit Isolated Current Output Card

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VME 4 Channel 16 Bit Isolated Current Output Card

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I. INTRODUCTION

GENERAL DESCRIPTION

The PAS 9819/AO provides four isolated, programmable current output channels with sixteen bit resolution on a 6U VME card. Each channel consists of a high speed Digital-to-Analog Converter (DAC), followed by a high power operational amplifier. The output amplifier is configured to provide an output current that is proportional to the output voltage from the DAC. The output current range is positive to negative forty mAmps.

Each channel is electrically isolated from system ground and from each other. Separate +/-30 volt isolated power supplies are provided for each channel. Digital data and control signals for each DAC channel are transmitted through digital isolators in order to keep the two sides electrically separated.

The output channel connections are terminated on a DB37 connector mounted through the front panel.

The card can be used in VME systems with A16, A24, or A32 addressing, and data writes of 16 and 32 bits are supported. DIP switches are used to configure the width of the address bus, and the instruction type specifies the data bus width. A board identifier PROM, control and status register, and a 32-bit test register are also provided.

Card Features: PAS 9819/AO

- ♣ 4 independent DAC channels with 16 bit programmable current outputs
- ♣ +/- 40 mAmp current output
- ♣ Binary Two's Complement data format
- ♣ DAC's reset to zero during power up or software reset
- ♣ Readback register for each channel provides the last data value that was loaded into the DAC
- ♣ Output slew rate of TBD mAmp per uSec
- ♣ Settling time of TBD uSec to 0.1% FSR
- ♣ Output signals terminate on a DB37 connector at the front panel
- ♣ VME 6U form factor; 233 mm x 160 mm card size
- ♣ VME access: D32, D16, A32, A24, A16 Slave
- ♣ No VME Interrupts
- ♣ VME SYSFAIL asserts on power up, jumper selectable
- ♣ Board Identifier PROM (Board ID is VMEIDPAS9819AOA0)
- ♣ Pass, Fail and Access LEDs on the front panel
- ♣ Simultaneous DAC update feature is program selectable.
- ♣ Loop back test registers allow verification of the VME bus interface.
- ♣ 32-bit VME interface allows two channels to be written with one transfer and provides twice the data transfer rate of 16 bit interfaces. 16 bit VME transfers are also supported.
- ♣ Each current output channel is powered by a separate, isolated, +/-30 volt DC-to-DC converter.
- ♣ Data and control signals are transmitted through digital isolators.
- ♣ Operating temperature range 0 to 60 degrees Celsius

II. SPECIFICATIONS

Electrical Specifications

Number of Channels	4 Analog Outputs
Resolution	16 bits
Output Current	+/- 40 mAmps
LSB bit weight	1.22 uAmp
Settling Time	TBD uSec to 0.1%(typ)

Standard Card

DAC Integral Nonlinearity T min. to T max.	+/- 4 LSB (max.) +/- 5 LSB (max.)
DAC Differential Nonlinearity T min to T max.	+/- 3 LSB (max.) +/- 4 LSB (max.)

Zero Error	+/- 2 LSB (adjustable to zero)
Gain Error	+/- 0.05 % FS (adjustable to zero)

Card Power Requirements (Backplane power supplies)	5 Volts @ 4 Amps, (typ) - TBD
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Environmental Specifications

Operating Temperature Range	0 to 60 degrees Celsius
Storage Temperature Range	-20 to 85 degrees Celsius
Relative Humidity Range	20% to 80%, non-condensing

Physical Specifications

Dimensions	Form factor: Double (160 mm x 233 mm)
Weight	16 oz. (typ) - TBD
Connectors	2 ea. 96 position, (VME bus connectors) 1 ea. DB37 female (Analog Output connector)

TABLE 1
PLUGGABLE JUMPER DEFINITIONS

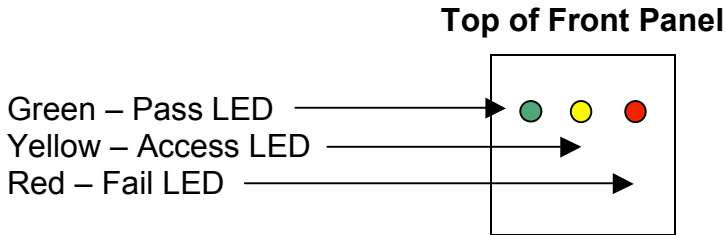
<u>Jumper #</u>	<u>Function</u>
J1 IN	SYSFAIL driven by bit 0 of CSR
J2, 1-2	16 MHz from backplane
J2, 2-3	16 MHz from oscillator
SW1-4	A11
SW1-5	A12
SW1-6	A13
SW1-7	A14
SW1-8	A15
SW2-1	A16
SW2-2	A17
SW2-3	A18
SW2-4	A19
SW2-5	A20
SW2-6	A21
SW2-7	A22
SW2-8	A23
SW3-1	A24
SW3-2	A25
SW3-3	A26
SW3-4	A27
SW3-5	A28
SW3-6	A29
SW3-7	A30
SW3-8	A31

TABLE 2
Address Modifiers

SW1-1	SW1-2	Address Modifiers	Address Space
Closed	Closed	09, 0D	Extended I/O
Open	Closed	39, 3D	Standard I/O
Open	Open	29, 2D	Short I/O

Front Panel LED Definitions

Three LED's are available at the front panel to indicate the board's status. The position of the LEDs is shown below.



The Fail LED powers up on, and is controlled with bit 0 of the control register. Writing a one to bit 0 will turn off this LED. The state of this LED is reflected in bit 0 of the status register. When the Fail LED is on, and J1 is installed, the SYSFAIL line will be driven on the VMEbus.

The Pass LED is controlled by bit 1 of the control register. This LED will be turned on by writing a one to bit 1, and it will power up turned off. Bit 1 in the status register reflects the state of this LED. Once the board has passed some initial power up tests this LED can be turned on to indicate successful completion of the power up sequence. The yellow, access LED will turn on anytime the board is accessed.

Connector Definitions

Two 96-position DIN connectors, (P1 and P2) are installed on the backplane end of the board to make the standard VME bus connection. A DB37 female connector, installed through the board's front panel, is available to provide access to the four analog output channels.

The pin definitions of the DB37 connector are defined on the following page.

TABLE 3
DB37 CONNECTOR

N/C	37	19	N/C
N/C	36	18	N/C
N/C	35	17	N/C
N/C	34	16	N/C
N/C	33	15	N/C
N/C	32	14	N/C
N/C	31	13	N/C
N/C	30	12	N/C
N/C	29	11	N/C
RETURN 0	28	10	OUTPUT 0
RETURN 1	27	9	OUTPUT 1
RETURN 2	26	8	OUTPUT 2
RETURN 3	25	7	OUTPUT 3
N/C	24	6	N/C
N/C	23	5	N/C
N/C	22	4	N/C
N/C	21	3	N/C
N/C	20	2	N/C
		1	N/C

III. PROGRAMMING INFORMATION

The 9819/AO card responds to word and longword writes and reads to the four Digital to Analog Converters (DAC's). The card also supports word writes and reads to the control and status register, and word reads of the board identifier PROM. A thirty two-bit test register is provided, and it responds to word and longword transfers. This register is useful for verifying the functionality of the VME bus interface. The card's memory map is shown below.

TABLE 4
PAS 9819/AO MEMORY MAP

00	00	V (56)	01
02	00	M (4D)	03
04	00	E (45)	05
06	00	I (49)	07
08	00	D (44)	09
0A	00	P (50)	0B
0C	00	A (41)	0D
0E	00	S (53)	0F
10	00	9 (39)	11
12	00	8 (38)	13
14	00	1 (31)	15
16	00	9 (39)	17
18	00	A (41)	19
1A	00	O (4F)	1B
1C	00	A (41)	1D
1E	00	0 (30)	1F
20	98	19	21
22	Control & Status	Control & Status	23
24	Reserved	Reserved	25
26	Reserved	Reserved	27
28	Test Register	Test Register	29
2A	Test Register	Test Register	2B
2C	Reserved	Reserved	2D
3E	Reserved	Reserved	3F
40	CH 0	CH 0	41
42	CH 1	CH 1	43
44	CH 2	CH 2	45
46	CH 3	CH 3	47
48	Reserved	Reserved	49
4A	Reserved	Reserved	4B
4C	Reserved	Reserved	4D
4E	Reserved	Reserved	4F

Board Identifier PROM (Base + 000H to 01FH) Read Only

The Board Identifier PROM is located starting at the board's base address plus 1, and continues to the base address plus 1F. Byte and word reads to the Identifier PROM are supported.

Only the least significant byte of a word read will contain valid data, and the most significant byte will contain FF. The ID PROM contains 16 ASCII characters that specify the board's model number and revision level. A write to the ID PROM location will handshake, but not transfer any data.

Fast ID Register (Base + 20H) Read Only

The fast ID register is located at the card's base address plus 20. Reads to this register will return the hex value 9819, which is the board's model number. Writing to this register will handshake, but not transfer any data.

Control and Status Register (Base +22H) Read / Write

The Control and Status Register (CSR) is located at the cards base address plus 23. Writes to the control register are used to set the states of the LED's and the SYSFAIL line, to control the simultaneous update function, and to software reset the board. The word format of the CSR is shown below.

TABLE 5

Control and Status Register

15	14 thru 5		4	3	2	1	0
Loop Back HT	Loop Back HT	Loop Back HT	Loop Back HT	SW Reset Pulse	Sim Updat HT	Pass LED HT	Fail LED LT

LT = Low True

HT = High True

Bit 0 of the CSR steers the Fail LED and the SYSFAIL line on the backplane, if J1 is installed. When the card is reset the Fail LED will come on, and the SYSFAIL line will be driven true. Writing a one to bit 0 will turn off the LED and the SYSFAIL line.

Bit 1 of the CSR controls the Pass LED. This LED will be turned off when the board is reset or when a zero is written to bit 1. Writing a one to bit 1 will turn on the LED.

Bit 2 of the CSR controls the simultaneous update feature. This function is disabled when the board is reset or when a zero is written to bit 2. When simultaneous update is disabled, the DAC outputs will updated when they are written.

Simultaneous update is used to update all of the DAC outputs at the same time, and is controlled with bit 2. The program sequence for updating the outputs simultaneously is described below in the section on the D to A converters.

Bit 3 of the CSR is used to generate a software reset pulse when it is written with a one. Writing a zero to bit 3 causes no action. This bit will always return a 0 when read. Following a software reset, the control and status register, test register and DAC registers all get reset to all zeros and the DACs all output zero mA.

Bits 4 through 7 of the CSR are loop back bits, and will return the value that was last written to them.

The power up or reset condition of the CSR is FF00, and indicates, that simultaneous update is disabled, the Pass LED is off and the Fail LED is on.

Test Register (Base + 28H) Read / Write

The 32-bit Test Register can be written to and read at the card's base address plus 28 (hex). This register supports word and long word transfers, and is useful for verifying the proper operation of the VME bus interface. Reading the register will return the value that was last written to it.

D to A Converters (Base + 40H) Read / Write

The four Digital to Analog Converters, (DAC's), are addressed starting at the board's base address plus 40 (hex). Binary Two's Complement is the data format written to the DAC's. Writing a value of 7FFF (hex) to a DAC produces positive full-scale output on that channel. Writing a value of 8000 (hex) produces negative full-scale output, and 0000 (hex) produces zero output.

Reading the DAC registers will return the value that was last written to them. The DACs used on this board have a serial data interface, and a CPLD is used to perform the parallel to serial conversion. When the DAC registers are read back, the value that is returned is from the parallel register in the CPLD.

Dual rank register pairs are used in the DAC's so that they can be updated simultaneously. Data is always written into the DAC's input register, which is the first register in the pair. If the simultaneous update feature is disabled, the second register, known as the DAC register, will also be updated during the write. This causes the output voltage for that channel to change immediately during the write.

When the DAC's are updated simultaneously, all of the DAC input registers are written, then the card is instructed to update all the DAC registers. This causes all of the outputs to change at the same time.

The following sequence is performed to cause the outputs to update simultaneously;

- 1) Bit 2 in the CSR is set to a one to disable the DAC registers from tracking the input registers,
- 2) All of the DAC input registers are written to,
- 3) Bit 2 in the CSR is set to zero. This causes all of the DAC outputs to update.

The Digital to Analog Converters can be written individually using word transfers, or in pairs using longword transfers. After a power up or software reset, the output voltage of all of the DAC's is 0.000 mAmp.

IV. CALIBRATION PROCEDURE (+/-40 mAmp)

Install the 9819/AO card in a VME chassis, and apply power. Allow the card to stabilize for approximately 5 minutes.

Offset Adjustment

The offset adjustment is performed before the gain adjustment to avoid interaction of adjustments. Write the hex value 0000 to the channel being calibrated, and adjust the zero potentiometer for a value of 0.0000 mAmps. The zero adjustments are defined in the Table 9, below.

Gain Adjustment

Write a hex value of 7FFF to the channel being calibrated, and adjust the gain potentiometer for a value of + 39.9988 mAmps. The gain adjustments are the defined in Table 9, below. Write the hex value 8000 to the channel being calibrated and verify the output current is -40.000 mAmps.

TABLE 6
OFFSET AND GAIN ADJUSTMENT POTS

Channel Number	P3 Pin Number	Offset Pot	Gain Pot	Channel Address
0	10	R11	R13	40
1	9	R22	R24	42
2	8	R33	R35	44
3	7	R44	R46	46