

PRELIMINARY

PAS 9912/AO
ENGINEERING SPECIFICATION

8 CHANNEL, 12 BIT, 15 VOLT
VME ANALOG OUTPUT CARD
PCB REVISION A

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8 Channel, 12 Bit, 15 Volt VME Analog Output Card

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8 Channel, 12 Bit, 15 Volt VME Analog Output Card

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I. INTRODUCTION

GENERAL DESCRIPTION

The PAS 9912/AO provides eight, twelve bit analog voltage output channels on a 6U VMEbus card. VME systems with A16, A24, or A32 addressing are supported, and data writes of 16 or 32 bits can be used. DIP switches are used to configure the width of the address bus and the data bus width is specified by the instruction type.

Two, quad high speed voltage output DACs, with 10 uSec settling times are used to provide a total of eight analog output channels. Eight high-power operational amplifiers buffer the DAC output signals and provide a gain of 1.5. The voltage output signals are available on the a and c rows of the P2 connector.

Four analog output ranges are available, under program control, which allows the card's output voltage to be tailored to your application. Bipolar ranges of ± 15 Volts and ± 7.5 Volts and unipolar ranges of 0 to 15 Volts and 0 to 7.5 Volts are supported. All output ranges provide a minimum of 20 milliamps of output current.

A pair of onboard DC to DC converters generate ± 15 Volts and ± 30 Volts from the 5 Volt backplane voltage. The DACs and reference voltages are powered by the ± 15 Volts and the power op-amps are powered by the ± 30 Volt supplies.

The power op-amps are Texas Instruments OPA452 and they will deliver 50 mA to the load. Refer to the data sheet for thermal considerations.

External synchronization signals can be connected to the P2 connector if required. These signals are described in section III under the Control and Status Register.

Additional features include a board identifier registers, control and status register, and DAC loop back registers.

Card Features: PAS 9912/AO

- 8 channels of analog voltage outputs, with a 12 bit D/A Converter per channel
- Software selectable ± 15 V, ± 7.5 V, 0 to 15V and 7.5V ranges @ 20 mAmp output current per channel
- All DACs are calibrated with a precision on board voltage reference
- Offset binary or two's complement data format software selectable
- DAC's reset to bipolar zero during power up reset
- Output impedance of 0.6 ohm
- Output slew rate of 2.2 Volts per uSec, Settling time of 10 uSec to 0.01%
- DACs have digital readback registers
- Two DACs can be updated with a single VME long word write
- Double buffered DACs can be updated simultaneously with software or external sync
- VME 6U form factor; 233 mm x 160 mm card size
- VME access: D32, D16; A32, A24, A16 Slave
- No VME Interrupts
- Optional VME SYSFAIL assert on power up, jumper selectable
- Pass, fail, and board access LEDs on the front panel
- Board Identifier Registers (Board ID is VMEID PAS9912/AO A0)
- Analog output signals terminate on the a and c rows of the P2 connector.
- External synchronization input and output signals can be connected to P2
- DACs are powered by ± 15 Volts from an on board DC-to-DC converter
- Output buffers are powered by ± 30 Volts from on-board DC to DC converters
- Operating temperature range -20 to 60 deg C

II. SPECIFICATIONS

Electrical Specifications

Number of Channels	8 Analog Outputs
Resolution	12 bits
Output Voltage	± 15 Volts, $\pm 7.5V$ 0 to 15 Volts, 0 to 7.5V
Output Current	± 15 mAmps (min)
Slew Rate	2.2 Volts / μ Sec
Settling Time	10 μ Sec (typ) to 0.01%
Integral Nonlinearity	± 1 LSB (max)
Differential Nonlinearity	± 1 LSB (max)
Zero Scale Error	± 2 LSB
Full Scale Error	± 4 LSB
Card Power Requirements	5 Volts @ TBD Amp, (typ)

Environmental Specifications

Operating Temperature Range	-20 to 60 degrees C.
Storage Temperature Range	-40 to 70 degrees C.
Relative Humidity Range	20% to 80%, non-condensing

Physical Specifications

Dimensions	Form factor: Double (160 mm x 233 mm)
Weight	16 oz. (typ)
Connectors	2 ea. 96 position, (VME bus connectors) Analog Outputs terminate on the a and c row of P2

Switches and Jumper Plug Definitions

The PAS 9912/AO card contains three eight position DIP switches, one three position DIP switch, and one jumper plug. The three eight position DIP switches are used to set the card's VME address and are defined in Table 1 on the following page. When a switch is closed or on, the corresponding address bit must be low to select the card's address. When a switch is open or off, the corresponding address bit must be high.

Switches SW4-1 and 2 are used to select the card's operating environment; A16, A24, or A32. The setting of these switches is defined in Table 2 on page 9.

Switch SW4-3 is used to enable the software reset function when it is open or off. Software reset is disabled when SW4-3 is closed or on. For more information on the software reset function, see the software reset register in the programming information section.

Jumper plug 1 allows bit zero of the CSR to control the SYSFAIL line, when it is installed. For more information see the CSR description in the programming section.

TABLE 1
SWITCH AND JUMPER DEFINITIONS

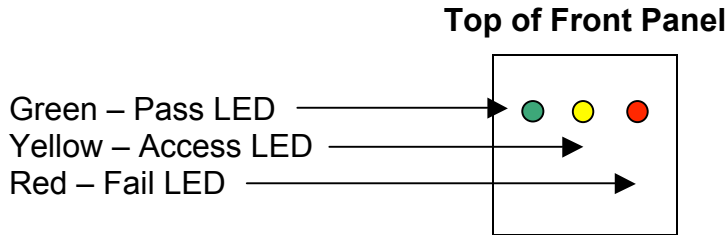
Switch #	Function
SW1-1	A8
SW1-2	A9
SW1-3	A10
SW1-4	A11
SW1-5	A12
SW1-6	A13
SW1-7	A14
SW1-8	A15
SW2-1	A16
SW2-2	A17
SW2-3	A18
SW2-4	A19
SW2-5	A20
SW2-6	A21
SW2-7	A22
SW2-8	A23
SW3-1	A24
SW3-2	A25
SW3-3	A26
SW3-4	A27
SW3-5	A28
SW3-6	A29
SW3-7	A30
SW3-8	A31

TABLE 2
SWITCH DEFINITIONS

SW4-1	SW4-2	Address Modifiers	Address Space
Closed	Closed	09, 0D	Extended
Open	Closed	39, 3D	Standard
Open	Open	29, 2D	Short

Front Panel LED Definitions

Three LED's are available at the front panel to indicate the board's status. The position of the LEDs is shown below.



The Fail LED powers up on, and is controlled with bit 0 of the Control and Status register (CSR). Writing a one to bit 0 will turn off this LED. The state of this LED is reflected in bit 0 of the CSR. When the Fail LED is on, and JP1 is installed, the SYSFAIL line will be driven on the VMEbus.

The Pass LED is controlled by bit 1 of the CSR. This LED will be turned on by writing a one to bit 1, and it will power up turned off. Bit 1 in the CSR reflects the state of this LED. Once the board has passed some initial power up tests this LED can be turned on to indicate successful completion of the power up sequence.

The yellow, access LED will turn on anytime the board is accessed.

Connector Definitions

Two 96-position DIN connectors, (P1 and P2) are installed on the backplane end of the board to make the standard VME bus connection. The analog output signals and the external sync connections are made through the a and c rows of the P2 connector. The output signal pin definitions of P2 are defined below.

TABLE 3

P2 Connector

AGND	P2a1	P2c1	OUTPUT 0
AGND	P2a2	P2c2	OUTPUT 1
AGND	P2a3	P2c3	OUTPUT 2
AGND	P2a4	P2c4	OUTPUT 3
AGND	P2a5	P2c5	OUTPUT 4
AGND	P2a6	P2c6	OUTPUT 5
AGND	P2a7	P2c7	OUTPUT 6
AGND	P2a8	P2c8	OUTPUT 7
N/C-See Note	P2a9	P2c9	N/C
N/C	P2a10	P2c10	N/C
N/C	P2a11	P2c11	N/C
N/C	P2a12	P2c12	N/C
N/C	P2a13	P2c13	N/C
N/C	P2a14	P2c14	N/C
N/C	P2a15	P2c15	N/C
N/C	P2a16	P2c16	N/C
N/C	P2a17	P2c17	N/C
N/C	P2a18	P2c18	N/C
N/C	P2a19	P2c19	N/C
N/C	P2a20	P2c20	N/C
N/C	P2a21	P2c21	N/C
N/C	P2a22	P2c22	N/C
N/C	P2a23	P2c23	N/C
N/C	P2a24	P2c24	N/C
N/C	P2a25	P2c25	N/C
N/C	P2a26	P2c26	N/C
N/C	P2a27	P2c27	N/C
N/C	P2a28	P2c28	N/C
N/C	P2a29	P2c29	N/C
Ext-Sync	P2a30	P2c30	N/C
N/C	P2a31	P2c31	N/C
GND	P2a32	P2c32	N/C

Note 1: N/C means no connection.

III. PROGRAMMING INFORMATION

The 9912/AO card responds to word and long-word writes and reads to the eight Digital to Analog Converters (DAC's). The card also supports word writes and reads to the control and status register, and word reads of the board identifier registers. The card's memory map is shown below.

TABLE 4
PAS 9915/AO MEMORY MAP

00	00	V (56)	01
02	00	M (4D)	03
04	00	E (45)	05
06	00	I (49)	07
08	00	D (44)	09
0A	00	P (50)	0B
0C	00	A (41)	0D
0E	00	S (53)	0F
10	00	9 (39)	11
12	00	9 (39)	13
14	00	1 (31)	15
16	00	2 (32)	17
18	00	A (41)	19
1A	00	O (4F)	1B
1C	00	A (41)	1D
1E	00	0 (30)	1F
20	99	12	21
22	Control & Status	Control & Status	23
24	Reserved	Reserved	25
26	Reserved	Reserved	27
28	Reserved	Reserved	29
2A	SW Sync	SW Sync	2B
2C	Reserved	Reserved	2D
2E	Reserved	Reserved	2F
30	Reserved	Reserved	31
□	Through	Through	□
3E	Reserved	Reserved	3F

Table continues below

Table continued from page 12

40	DAC Channel 0	41
42	DAC Channel 1	43
44	DAC Channel 2	45
46	DAC Channel 3	47
48	DAC Channel 4	49
4A	DAC Channel 5	4B
4C	DAC Channel 6	4D
4E	DAC Channel 7	4E
50	Reserved	51
52	Reserved	53
54	Reserved	55
56	Reserved	57
58	Reserved	59
5A	Reserved	5B
5C	Reserved	5D
5E	Reserved	5F
60	Reserved	61
62	Reserved	63
64	Reserved	65
66	Reserved	67
68	Reserved	69
6A	Reserved	6B
6C	Reserved	6D
6E	Reserved	6F
70	Reserved	71
72	Reserved	73
74	Reserved	75
76	Reserved	77
78	Reserved	79
7A	Reserved	7B
7C	Reserved	7D
7E	Reserved	7F

Board Identifier Registers (Base Address + 00H to 1EH) Read Only

The Board Identifier Registers are located starting at the board's base address plus 0, and continues to the base address plus 1E. Byte and word reads to the Identifier PROM are supported.

Only the least significant byte of a word read will contain valid data, and the most significant byte will contain 00. The ID Registers contains 16 ASCII characters that specify the board's model number and revision level. A write to the ID PROM location will handshake, but not transfer any data.

Fast ID Register (Base Address + 20H) Read Only

The fast ID register is located at the card's base address plus 20. Reads to this register will return the hex value 9912, which is the board's model number. Writing this register will handshake, but not transfer any data.

Control and Status Register (Base address + 22) Read/Write

The Control and Status Register (CSR) is located at the cards base address plus twenty-two. Writes to the CSR are used to determine what conditions will update the DACs, select the data format and output voltage range, and software reset the board. The format of the CSR is shown below.

TABLE 5
CSR WORD FORMAT

7	6	5	4	3	2	1	0
Loop Back	SW Reset	Bipolar Unipolar	Output Range	Update Mode	Update Mode	Pass LED	Fail LED
15	14	13	12	11	10	9	8
Loop Back	Loop Back	Loop Back	Loop Back	Sync Status	Sync In	Sync Out	Enable Sync

Bit 0 of the CSR steers the Fail LED and the SYSFAIL line on the backplane, if J1 is installed. When the card is reset the Fail LED will come on, and the SYSFAIL line will be driven true. Writing a one to bit 0 will turn off the LED and the SYSFAIL line.

Bit 1 of the CSR controls the Pass LED. This LED will be turned off when the board is reset or when a zero is written to bit 1. Writing a one to bit 1 will turn on the LED.

Bits 2 and 3 of the CSR determine when the DAC's output registers will be updated, and the states of these bits are defined in the table below.

TABLE 6
DAC Update Mode

Bit 3	Bit 2	DAC update mode
0	0	DACs update when they are written
0	1	DACs update when the external sync signal is low
1	0	DACs update when the external sync signal is high
1	1	DACs update with a software sync.

Bit 4 and 5 of the CSR determine the card's output voltage range and if the output range is unipolar or bipolar. Bit 4 selects the range, and bit 5 selects unipolar or bipolar. The states of these bits are defined in the following table.

TABLE 7
Output Voltage Range

Bit 5	Bit 4	Output Voltage Range
0	0	± 15 Volts
0	1	± 7.5 Volts
1	0	0 to 15 Volts
1	1	0 to 7.5 Volts

When card is configured for bipolar outputs, 2's complement data is used and unipolar output configurations use offset binary data. Refer to section on the Digital-to-Analog Converters for more information on the data formats.

Bit 6 in the Control Register controls the software reset function when enabled by SW4-3 being open. When bit 6 is written with a one with the reset enabled, the reset pulse will be generated. Software reset causes all the DACs to reset to zero volts and clears the CSR to all zeros. When the software reset function is disabled, bit 632 has no function, other than to loop back the value that was written last.

Bit 7 of the CSR is a loop back bit, and will return the value that was last written.

Bit 8 of the CSR controls the Enable Sync Output signal. Writing a one to this bit will enable the sync output buffer, Writing a zero will disable the sync output buffer. Reading this bit will return the value that was last written.

Bit 9 of the CSR controls the Sync Output signal when the sync output buffer is enabled with bit 8 of the CSR. Writing a one will cause a high TTL level voltage on the external sync line. Writing a zero will cause a low TTL level voltage on the external sync line. Reading this bit will return the value last written.

Bit 10 of the CSR monitors the state of the external sync line and is a read only bit. When this bit returns a one, it indicates a high level TTL level on the external sync line. When this bit returns a zero, it indicates a low level TTL voltage on the external sync line. When the external sync output buffer is enabled on this card with bit 8 of the CSR, then bit 9 and 10 of the CSR will always agree.

Bit 11 of the CSR is the synchronization status bit, and returns a 1 when the condition that causes the DACs to be updated has occurred. The sync status bit resets after the CSR is read. When the card is configured to update whenever a DAC is written, this bit will always return a zero, since the update event is not required. If the card is configured to update the DACs with an external or software sync signal, then this bit will return a 1 when the trigger event occurs, and will reset to 0, after the CSR is read.

The power up or reset condition of the Control and Status Register is 0000, and indicates the +/- 15 Volt output range is selected with 2's compliment data format, and the DACs will update when they are written.

Software Sync Register (Base Address + 2A) Read/Write

The Software Sync Register is located at the boards base address plus 2A. Writing to this location causes the DAC output registers to be updated, if the software sync mode was selected with the CSR. Reading the software sync register will return a value of 0000.

8 Digital to Analog Converters

The eight D-to-A Converters (DACs) can be written to starting at the board's base address plus 40 (hex). Binary Two's Complement or Offset Binary data can be written to the DACs depending on the state of bit five in the Control and Status Register. Two's complement data should be used with bipolar outputs, so that the code required to produce a negative voltage can be determined by taking the 2's complement of the code that produces a positive voltage of the same magnitude. For the bipolar Analog Output configuration of this card, using Two's Complement data a digital word of 7FF gives positive full scale output, 800 hex gives negative full scale output Hex 000 produces bipolar zero output. All of the negative voltage codes have the MSB set to a one, so it represents the sign bit. The magnitude of positive full scale is always 1 LSB less than the magnitude of negative full scale, because of the one code required for zero.

Offset binary data should be used with unipolar outputs, since the sign of the data is always positive. A digital output word of FFF provides positive full scale in this configuration. Zero volts are produced with a digital word of 000, and half scale occurs at 800 hex.

Dual rank registers are used in the DAC's and data is always written into the DAC's input register. If the simultaneous update feature is disabled, the DAC register will also be updated during this write. If the DAC's are to be updated simultaneously, then the following sequence should be performed;

- 1) Bits 2 and 3 in the Control Register are set to select the condition that will update the DAC registers
- 2) all of the DACs are written to,
- 3) when the synchronization pulse occurs, all of the DACs will be updated.
- 4) The state of the update signal can be monitored by reading bits ten and eleven in the status register.

The Digital to Analog Converters can be written to individually using word transfers, or in pairs using longword transfers. During a power up reset, all of the DAC outputs will be set to mid scale. This is 0.000 Volts, since the card resets to the +/- 15 Volt range.

IV. CALIBRATION PROCEDURE

- 1) Install the 9912/AO card in a VME chassis, and allow the card to stabilize for approximately 2 minutes.
- 2) All of the DACs on this card are connected to a common voltage reference, and only two adjustments are required to adjust the entire card.
- 3) Positive reference voltage adjustment.
Monitor the positive reference voltage from TP1 to analog ground at TP2.
Adjust R6 for a value of 10.000 Volts.
- 4) Negative reference voltage adjustment.
Monitor the negative reference voltage from TP3 to analog ground at TP2.
Adjust R7 for a value of -10.000 Volts.