

PRELIMINARY

---

---

**PAS 9915/AO**  
**ENGINEERING SPECIFICATION**

---

---

**32 CHANNEL, 12 BIT**  
**VME ANALOG OUTPUT CARD**  
**PCB REVISION A (08/24/07)**

Additional copies of this manual or other Precision Analog Systems (PAS) literature may be obtained from:

Precision Analog Systems Co.  
7540 NW 5<sup>th</sup> Street - Suite 2  
Plantation, Florida 33317  
Phone: (954) 587-0668  
Fax: (954) 587-0665  
E-mail: [info@precisionanalog.com](mailto:info@precisionanalog.com)

The information in this document is subject to change without notice.

PAS makes no warranty of any kind with regard to this material, including, but not limited to, the implied warranties of merchantability and fitness for a particular purpose. Although extensive editing and reviews are performed before release, PAS assumes no responsibility for any errors that may exist in this document. No commitment is made to update or keep current the information contained in this document.

PAS does not assume any liability arising out of the application or use of any product or circuit described herein, nor is any license conveyed under any patent rights or any rights of others.

PAS assumes no responsibility resulting from omissions or errors in this manual, or from the use of information contained herein.

PAS reserves the right to make any changes, without notice, to this product to improve reliability, performance, function or design.

All rights reserved.

# 32 Channel 12 Bit VME Analog Output Card

## TABLE OF CONTENTS

Section	Title	Page
I	<b>INTRODUCTION</b>	5
	General Description	5
	Card Features	6
II	<b>SPECIFICATIONS</b>	7
	Electrical Specifications	7
	Environmental Specifications	7
	Physical Specifications	7
	Switch & Jumper Pug Definitions	8
	Front Panel LED Definitions	10
	Connector Definitions	10
III	<b>PROGRAMMING INFORMATION</b>	12
	Board Identifier PROM	14
	Fast ID Register	14
	Control and Status Register	14
	Software Sync Register	16
	32 Digital to Analog Converters	17
IV	<b>CALIBRATION PROCEDURE</b>	18

# 32 Channel 12 Bit VME Analog Output Card

## LIST OF TABLES

Table	Title	Page
1	Switch and Jumper Definitions	9
2	Switch Definitions	9
3	P2 Connectors	11
4	Memory Map	12
5	CSR Word Format	14
6	DAC Update Mode	14
7	Output Voltage Range	15

# I. INTRODUCTION

## GENERAL DESCRIPTION

The PAS 9915/AO provides thirty-two, twelve bit analog voltage output channels on a 6U VMEbus card. VME systems with A16, A24, or A32 addressing are supported, and data writes of 16 or 32 bits can be used. DIP switches are used to configure the width of the address bus and the data bus width is specified by the instruction type.

Eight, quad high speed voltage output DACs, with 10 uSec settling times are used to provide a total of thirty two analog output channels. The voltage output signals are available on the a and c rows of the P2 connector.

Six analog output ranges are available, under program control, which allows the card's output voltage to be tailored to your application. Bipolar ranges from +/- 10 volts to +/- 2.5 volts and unipolar ranges from 0 to 10 volts to 0 to 2.5 volts are supported. All output ranges provide a minimum of 10 milliamps of output current.

External synchronization signals can be connected to the P2 connector if required. These signals are selected with jumper plugs as described in section II.

Additional features include a board identifier PROM, control and status register, and DAC loop back registers.

### **Card Features: PAS 9915/AO**

- 32 channels of analog voltage outputs, with a 12 bit D/A Converter per channel
- Software selectable +/- 10 V, +/- 5V, 0-10V, 0 to 5V, ranges @ 10 mAmp output current per channel
- All DACs are calibrated with a precision on board voltage reference
- Offset binary or two's complement data format software selectable
- DAC's reset to bipolar zero during power up reset
- Output impedance of 0.6 ohm
- Output slew rate of 2.2 Volts per uSec, Settling time of 10 uSec to 0.01%
- DACs have digital readback registers
- Two DACs can be updated with a single VME long word write
- Double buffered DACs can be updated simultaneously with software or external sync
- VME 6U form factor; 233 mm x 160 mm card size
- VME access: D32, D16; A32, A24, A16 Slave
- No VME Interrupts
- Optional VME SYSFAIL assert on power up, jumper selectable
- Pass, fail, and board access LEDs on the front panel
- Board Identifier PROM (Board ID is VMEID PAS9915/AO A0)
- Analog output signals terminate on the a and c rows of the P2 connector.
- External synchronization input and output signals can be connected to P2 through jumper plugs.
- DACs are powered by +/- 15 Volts from an on board DC-to-DC converter
- Operating temperature range 0 to 60 deg C.

## II. SPECIFICATIONS

### Electrical Specifications

Number of Channels	32 Analog Outputs
Resolution	12 bits
Output Voltage	+/- 10 Volts, +/- 5 Volts 0 to 10 Volts, 0 to 5 Volts
Output Current	+/- 10 mAmps (min)
Slew Rate	2.2 Volts 1 uSec
Settling Time	10 uSec (typ) to 0.01%
Integral Nonlinearity	+/- 1 LSB (max)
Differential Nonlinearity	+/- 1 LSB (max)
Zero Scale Error	+/- 2 LSB
Full Scale Error	+/- 2 LSB
Card Power Requirements	5 Volts @ TBD Amp, (typ)

### Environmental Specifications

Operating Temperature Range	0 to 60 degrees C.
Storage Temperature Range	-20 to 85 degrees C.
Relative Humidity Range	20% to 80%, non-condensing

### Physical Specifications

Dimensions	Form factor: Double (160 mm x 233 mm)
Weight	12 oz. (typ)
Connectors	2 ea. 96 position, (VME bus connectors) Analog Outputs terminate on the a and c row of P2

## Switches and Jumper Plug Definitions

The PAS 9915/AO card contains three eight position DIP switches, one three position DIP switch, and one jumper plug. The three eight position DIP switches are used to set the card's VME address and are defined in Table 1 below. When a switch is closed or on, the corresponding address bit must be low to select the card's address. When a switch is open or off, the corresponding address bit must be high.

Switches SW4-1 and 2 are used to select the card's operating environment; A16, A24, or A32. The setting of these switches is defined in Table 2 on page 9.

Switch SW4-3 is used to enable the software reset function when it is open or off. Software reset is disabled when SW4-3 is closed or on. For more information on the software reset function, see the software reset register in the programming information section.

Jumper plug 1 allows bit zero of the CSR to control the SYSFAIL line, when it is installed. For more information see the CSR description in the programming section.

Jumper plug 2 and 3 are used to connect or disconnect the external sync signal to or from the P2 backplane connector.

When they are position 2 to 3 the external sync function is disabled. Selecting pins 1 to 2 enables the external sync function. The definition of these jumpers is show below.

JP2, 1 to 2	P2a30 to external sync
JP2, 2 to 3	P2a30 to analog ground
JP3, 1 to 2	P2a32 to digital ground
JP3, 2 to 3	P2a32 to analog ground

When external sync is selected, both jumpers should be moved to position 1 to 2. This allows the return current from the sync signal to flow through the digital ground and not the analog ground.

**TABLE 1**  
**SWITCH AND JUMPER DEFINITIONS**

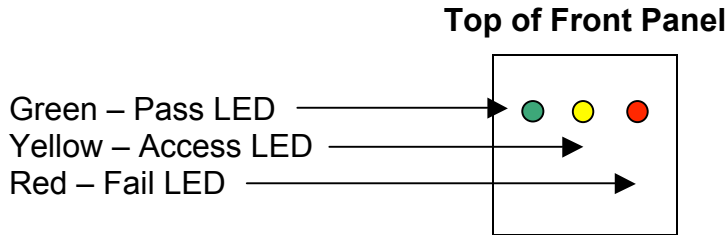
<b>Switch #</b>	<b>Function</b>
SW1-1	A8
SW1-2	A9
SW1-3	A10
SW1-4	A11
SW1-5	A12
SW1-6	A13
SW1-7	A14
SW1-8	A15
SW2-1	A16
SW2-2	A17
SW2-3	A18
SW2-4	A19
SW2-5	A20
SW2-6	A21
SW2-7	A22
SW2-8	A23
SW3-1	A24
SW3-2	A25
SW3-3	A26
SW3-4	A27
SW3-5	A28
SW3-6	A29
SW3-7	A30
SW3-8	A31

**TABLE 2**  
**SWITCH DEFINITIONS**

<b>SW4-1</b>	<b>SW4-2</b>	<b>Address Modifiers</b>	<b>Address Space</b>
Closed	Closed	09, 0D	Extended
Open	Closed	39, 3D	Standard
Open	Open	29, 2D	Short

## Front Panel LED Definitions

Three LED's are available at the front panel to indicate the board's status. The position of the LEDs is shown below.



The Fail LED powers up on, and is controlled with bit 0 of the LED register. Writing a one to bit 0 will turn off this LED. The state of this LED is reflected in bit 0 of the LED register. When the Fail LED is on, and JP2 is installed, the SYSFAIL line will be driven on the VMEbus.

The Pass LED is controlled by bit 1 of the LED register. This LED will be turned on by writing a one to bit 1, and it will power up turned off. Bit 1 in the LED register reflects the state of this LED. Once the board has passed some initial power up tests this LED can be turned on to indicate successful completion of the power up sequence.

The yellow, access LED will turn on anytime the board is accessed.

## Connector Definitions

Two 96-position DIN connectors, (P1 and P2) are installed on the backplane end of the board to make the standard VME bus connection. The analog output signals and the external sync connections are made through the a and c rows of the P2 connector. The output signal pin definitions of P2 are defined below.

**TABLE 3**  
**P2 Connector**

AGND	P2a1	P2c1	OUTPUT 0
AGND	P2a2	P2c2	OUTPUT 1
AGND	P2a3	P2c3	OUTPUT 2
AGND	P2a4	P2c4	OUTPUT 3
AGND	P2a5	P2c5	OUTPUT 4
AGND	P2a6	P2c6	OUTPUT 5
AGND	P2a7	P2c7	OUTPUT 6
AGND	P2a8	P2c8	OUTPUT 7
AGND	P2a9	P2c9	OUTPUT 8
AGND	P2a10	P2c10	OUTPUT 9
AGND	P2a11	P2c11	OUTPUT 10
AGND	P2a12	P2c12	OUTPUT 11
AGND	P2a13	P2c13	OUTPUT 12
AGND	P2a14	P2c14	OUTPUT 13
AGND	P2a15	P2c15	OUTPUT 14
AGND	P2a16	P2c16	OUTPUT 15
AGND	P2a17	P2c17	OUTPUT 16
AGND	P2a18	P2c18	OUTPUT 17
AGND	P2a19	P2c19	OUTPUT 18
AGND	P2a20	P2c20	OUTPUT 19
AGND	P2a21	P2c21	OUTPUT 20
AGND	P2a22	P2c22	OUTPUT 21
AGND	P2a23	P2c23	OUTPUT 22
AGND	P2a24	P2c24	OUTPUT 23
AGND	P2a25	P2c25	OUTPUT 24
AGND	P2a26	P2c26	OUTPUT 25
AGND	P2a27	P2c27	OUTPUT 26
AGND	P2a28	P2c28	OUTPUT 27
AGND	P2a29	P2c29	OUTPUT 28
AGND-Note 1	P2a30	P2c30	OUTPUT 29
AGND	P2a31	P2c31	OUTPUT 30
AGND-Note 1	P2a32	P2c32	OUTPUT 31

Note 1: These pins can be used for the external sync signals. Refer to the jumper plug section for more information.

### III. PROGRAMMING INFORMATION

The 9915/AO card responds to word and long-word writes and reads to the thirty-two Digital to Analog Converters (DAC's). The card also supports word writes and reads to the control and status register, and word reads of the board identifier PROM. The card's memory map is shown below.

**TABLE 4**  
**PAS 9915/AO MEMORY MAP**

00	00	V (56)	01
02	00	M (4D)	03
04	00	E (45)	05
06	00	I (49)	07
08	00	D (44)	09
0A	00	P (50)	0B
0C	00	A (41)	0D
0E	00	S (53)	0F
10	00	9 (39)	11
12	00	9 (39)	13
14	00	1 (31)	15
16	00	5 (35)	17
18	00	A (41)	19
1A	00	O (4F)	1B
1C	00	A (41)	1D
1E	00	0 (30)	1F
20	99	15	21
22	Control & Status	Control & Status	23
24	Reserved	Reserved	25
26	Reserved	Reserved	27
28	Reserved	Reserved	29
2A	SW Sync	SW Sync	2B
2C	Reserved	Reserved	2D
2E	Reserved	Reserved	2F
30	Reserved	Reserved	31
□	Through	Through	□
3E	Reserved	Reserved	3F

Table continues below

Table continued from page 11

40	DAC Channel 0	41
42	DAC Channel 1	43
44	DAC Channel 2	45
46	DAC Channel 3	47
48	DAC Channel 4	49
4A	DAC Channel 5	4B
4C	DAC Channel 6	4D
4E	DAC Channel 7	4E
50	DAC Channel 8	51
52	DAC Channel 9	53
54	DAC Channel 10	55
56	DAC Channel 11	57
58	DAC Channel 12	59
5A	DAC Channel 13	5B
5C	DAC Channel 14	5D
5E	DAC Channel 15	5F
60	DAC Channel 16	61
62	DAC Channel 17	63
64	DAC Channel 18	65
66	DAC Channel 19	67
68	DAC Channel 20	69
6A	DAC Channel 21	6B
6C	DAC Channel 22	6D
6E	DAC Channel 23	6F
70	DAC Channel 24	71
72	DAC Channel 25	73
74	DAC Channel 26	75
76	DAC Channel 27	77
78	DAC Channel 28	79
7A	DAC Channel 29	7B
7C	DAC Channel 30	7D
7E	DAC Channel 31	7F

### **Board Identifier PROM (Base Address + 00H to 1EH) Read Only**

The Board Identifier PROM is located starting at the board's base address plus 0, and continues to the base address plus 1E. Byte and word reads to the Identifier PROM are supported.

Only the least significant byte of a word read will contain valid data, and the most significant byte will contain 00. The ID PROM contains 16 ASCII characters that specify the board's model number and revision level. A write to the ID PROM location will handshake, but not transfer any data.

### **Fast ID Register (Base Address + 20H) Read Only**

The fast ID register is located at the card's base address plus 20. Reads to this register will return the hex value 9915, which is the board's model number. Writing this register will handshake, but not transfer any data.

### **Control and Status Register (Base address + 22) Read/Write**

The Control and Status Register (CSR) is located at the cards base address plus twenty-two. Writes to the CSR are used to determine what conditions will update the DACs, select the data format and output voltage range, and software reset the board. The format of the CSR is shown below.

**TABLE 5**  
**CSR WORD FORMAT**

7	6	5	4	3	2	1	0
Loop Back	SW Reset	Unipolar Bipolar	Output Range	Update Mode	Update Mode	Pass LED	Fail LED
15	14	13	12	11	10	9	8
Loop Back	Loop Back	Loop Back	Loop Back	Sync Status	Sync In	Sync Out	Enable Sync

**Bits 2 and 3** of the CSR determine when the DAC's output registers will be updated, and the states of these bits are defined in the table below.

**TABLE 6**  
**DAC Update Mode**

Bit 3	Bit 2	DAC update mode
0	0	DACs update when they are written
0	1	DACs update on the negative edge of the external sync signal
1	0	DACs update on the positive edge of the external sync signal
1	1	DACs update with a software sync.

**Bit 0** of the CSR steers the Fail LED and the SYSFAIL line on the backplane, if J1 is installed. When the card is reset the Fail LED will come on, and the SYSFAIL line will be driven true. Writing a one to bit 0 will turn off the LED and the SYSFAIL line.

**Bit 1** of the CSR controls the Pass LED. This LED will be turned off when the board is reset or when a zero is written to bit 1. Writing a one to bit 1 will turn on the LED.

**Bit 4 and 5** of the CSR determine the card's output voltage range and if the output range is unipolar or bipolar. Bit 4 selects the range, and bit 5 selects unipolar or bipolar. The states of these bits are defined in the following table.

**TABLE 7**  
**Output Voltage Range**

Bit 5	Bit 4	Output Voltage Range
0	0	$\pm 10$ Volts
0	1	$\pm 5.0$ Volts
1	0	0 to 10 Volts
1	1	0 to 5.0 Volts

When card is configured for bipolar outputs, 2's complement data is used and unipolar output configurations use offset binary data. Refer to section on the Digital-to-Analog Converters for more information on the data formats.

**Bit 6** in the Control Register controls the software reset function when enabled by SW4-3 being open. When bit 6 is written with a one with the reset enabled, the reset pulse will be generated. Software reset causes all the DACs to reset to zero volts and clears the CSR to all zeros. When the software reset function is disabled, bit 3 has no function, other than to loop back the value that was written last.

**Bit 7** of the CSR is a loop back bit, and will return the value that was last written.

**Bit 8** of the CSR controls the Enable Sync Output signal. Writing a one to this bit will enable the sync output buffer, Writing a zero will disable the sync output buffer. Reading this bit will return the value that was last written. This bit should only be used when external sync is selected with JP2.

**Bit 9** of the CSR controls the Sync Output signal when the sync output buffer is enabled with bit 8 of the CSR. Writing a one will cause a high TTL level voltage on the external sync line. Writing a zero will cause a low TTL level voltage on the external sync line. Reading this bit will return the value last written.

**Bit 10** of the CSR monitors the state of the external sync line and is a read only

bit. When this bit returns a one, it indicates a high level TTL level on the external sync line. When this bit returns a zero, it indicates a low level TTL voltage on the external sync line. When the external sync output buffer is enabled on this card with bit 8 of the CSR, then bit 9 and 10 of the CSR will always agree.

**Bit 11** of the CSR is the synchronization status bit, and returns a 1 when the condition that causes the DACs to be updated has occurred. The sync status bit resets after the CSR is read. When the card is configured to update whenever a DAC is written, this bit will always return a zero, since the update event is not required. If the card is configured to update the DACs with an external or software sync signal, then this bit will return a 1 when the trigger event occurs, and will reset to 0, after the CSR is read.

The power up or reset condition of the Control and Status Register is 0000, and indicates the +/- 10 Volt output range is selected with 2's complement data format, and the DACs will update when they are written.

#### **Software Sync Register (Base Address + 2A) Read/Write**

The Software Sync Register is located at the boards base address plus 2A. Writing to this location causes the DAC output registers to be updated, if the software sync mode was selected with the CSR. Reading the software sync register will return a value of 0000.

## 32 Digital to Analog Converters

The thirty-two D-to-A Converters (DACs) can be written to starting at the board's base address plus 40 (hex). Binary Two's Complement or Offset Binary data can be written to the DACs depending on the state of bit three in the Control and Status Register. Two's complement data should be used with bipolar outputs, so that the code required to produce a negative voltage can be determined by taking the 2's complement of the code that produces a positive voltage of the same magnitude. For the bipolar Analog Output configuration of this card, using Two's Complement data a digital word of 7FF gives positive full scale output, 800 hex gives negative full scale output Hex 000 produces bipolar zero output. All of the negative voltage codes have the MSB set to a one, so it represents the sign bit. The magnitude of positive full scale is always 1 LSB less than the magnitude of negative full scale, because of the one code required for zero.

Offset binary data should be used with unipolar outputs, since the sign of the data is always positive. A digital output word of FFF provides positive full scale in this configuration. Zero volts are produced with a digital word of 000, and half scale occurs at 800 hex.

Dual rank registers are used in the DAC's and data is always written into the DAC's input register. If the simultaneous update feature is disabled, the DAC register will also be updated during this write. If the DAC's are to be updated simultaneously, then the following sequence should be performed;

- 1) Bits 1 and 2 in the Control Register are set to select the condition that will update the DAC registers
- 2) all of the DACs are written to,
- 3) when the synchronization pulse occurs, all of the DACs will be updated.
- 4) The state of the update signal can be monitored by reading bit zero in the status register.

The Digital to Analog Converters can be written to individually using word transfers, or in pairs using longword transfers. During a power up reset, all of the DAC outputs will be set to mid scale. This is 0.000 Volts, since the card resets to the +/- 10 Volt range.

## IV. CALIBRATION PROCEDURE

- 1) Install the 9915/AO card in a VME chassis, and allow the card to stabilize for approximately 2 minutes.
- 2) All of the DACs on this card are connected to a common voltage reference, and only two adjustments are required to adjust the entire card.
- 3) Positive reference voltage adjustment.  
Monitor the positive reference voltage from TP1 to analog ground at TP2.  
Adjust R6 for a value of 10.000 Volts.
- 4) Negative reference voltage adjustment.  
Monitor the negative reference voltage from TP3 to analog ground at TP2.  
Adjust R7 for a value of -10.000 Volts.